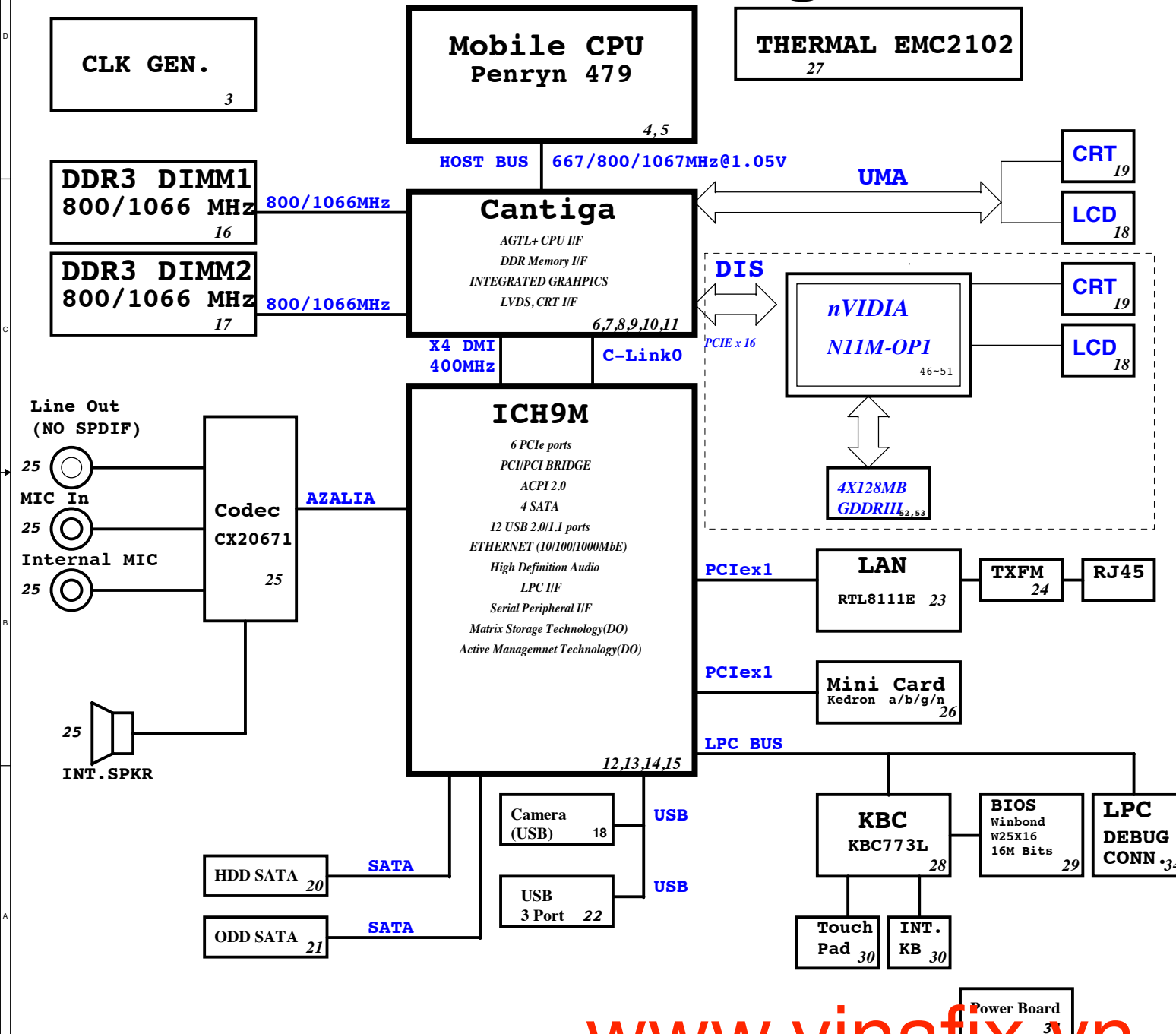


LB46E Block Diagram

Project code: 91.4HK01.A01

PCB P/N :

REVISION : 10307-sc



PCB STACKUP

TOP _____

VCC

S _____

S

END

BOTTOM _____

SYSTEM DC/DC	
TPS51125 37	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5
SYSTEM DC/DC	
TPS51218/RT9025 39	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S0
TPS51116 38	
DCBATOUT	1D5V_S3
TPS51116 38	
1D5V_S3	0D75V_S0
CPU DC/DC	
ISL6266A 36	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V
CHARGER	
BQ24745 41	
INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

<Core Design>

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,

Taipei Hsien 221, Taiwan, R.O.C.

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1 BLOCK DIAGRAM

Size

Document Number	
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A3

Date: Monday, December 27, 2010

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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default). 1 = Digital display Port and PCIE are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

NOTE:

- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
 - iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
- Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

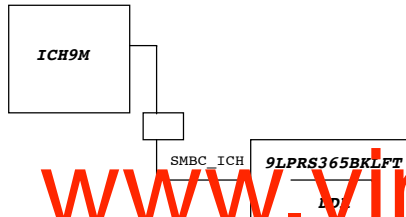
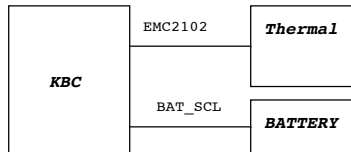
USB Table

USB	
Pair	Device
0	USB1
1	USB3
2	NC
3	MINIC1
4	WEBCAM
5	NC
6	NC
7	NC
8	NC
9	USB2
10	NC
11	NC

PCIE Routing

LANE1	RTL8111E
LANE2	MiniCard WLAN
LANE3	NC
LANE4	NC
LANE5	NC
LANE6	NC

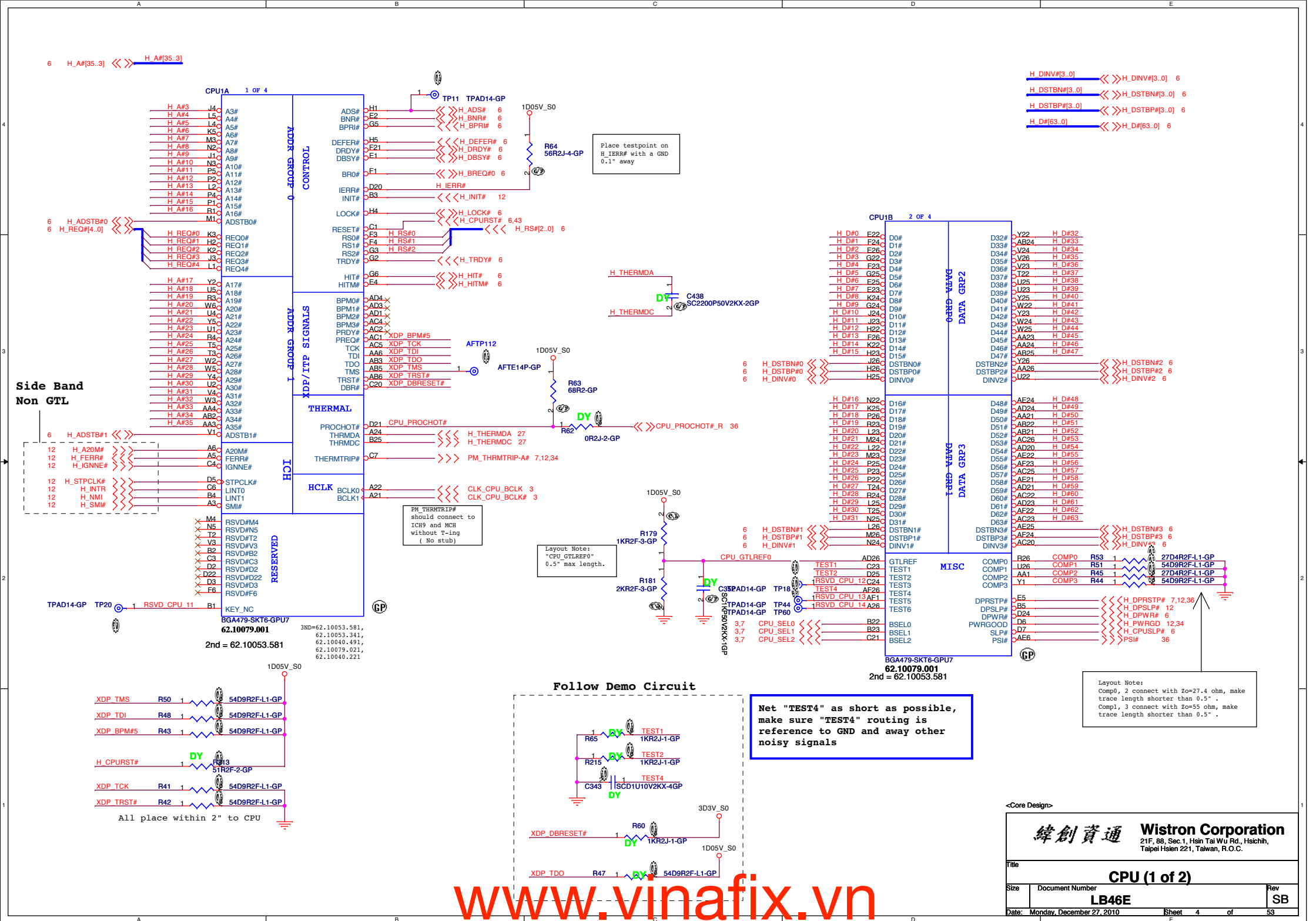
SMBus

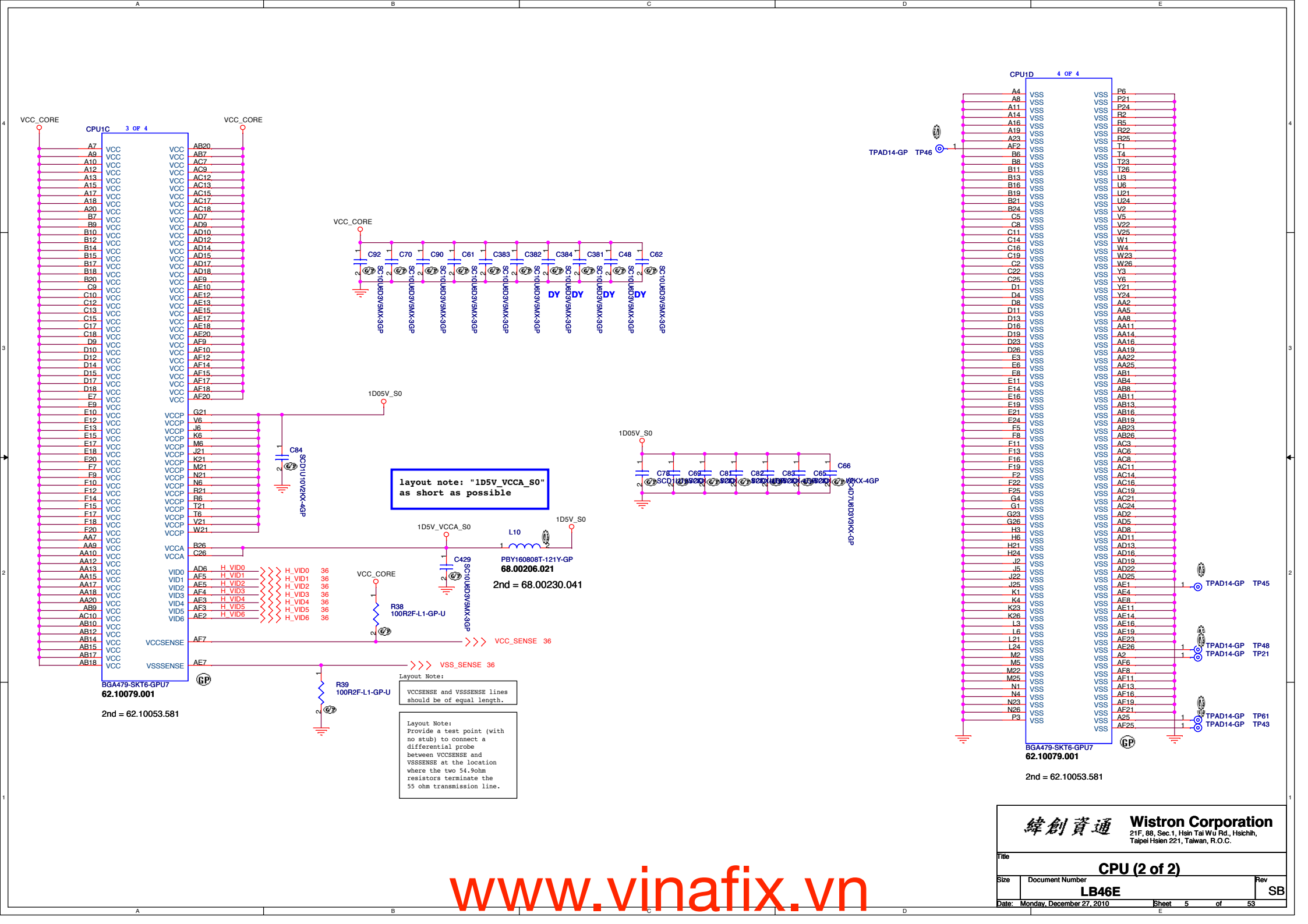


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layout note: "1D5V_VCCA_S0"
as short as possible

Layout Note:
VCCSENSE and VSSSENSE lines
should be of equal length.

Layout Note:
Provide a test point (with
no stub) to connect a
differential probe
between VCCSENSE and
VSSSENSE at the location
where the two 54.9ohm
resistors terminate the
55 ohm transmission line.

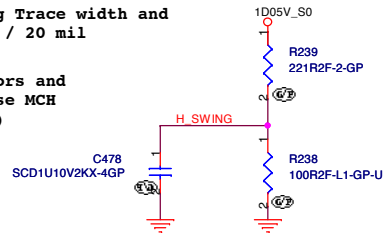
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Title			CPU (2 of 2)	
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LB46E				
Date: Monday, December 27, 2010	Sheet	5	of	53

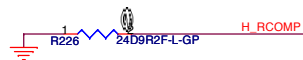
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H_SWING routing Trace width and Spacing use 10 / 20 mil

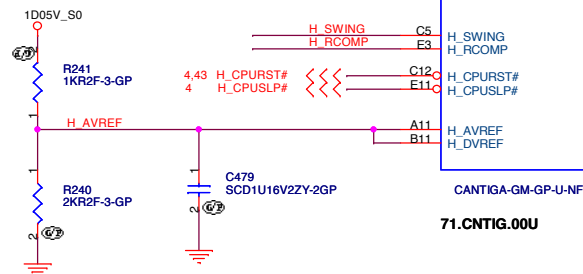
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



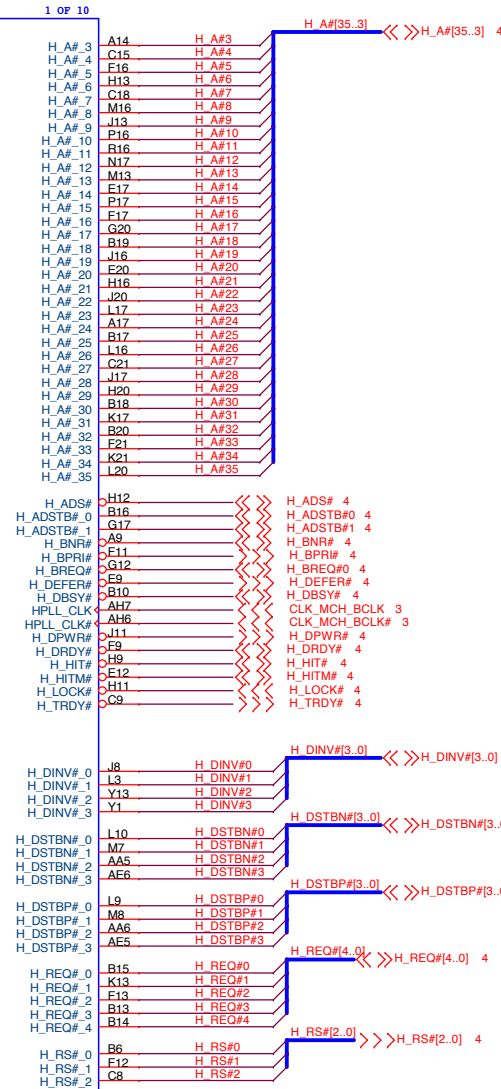
H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



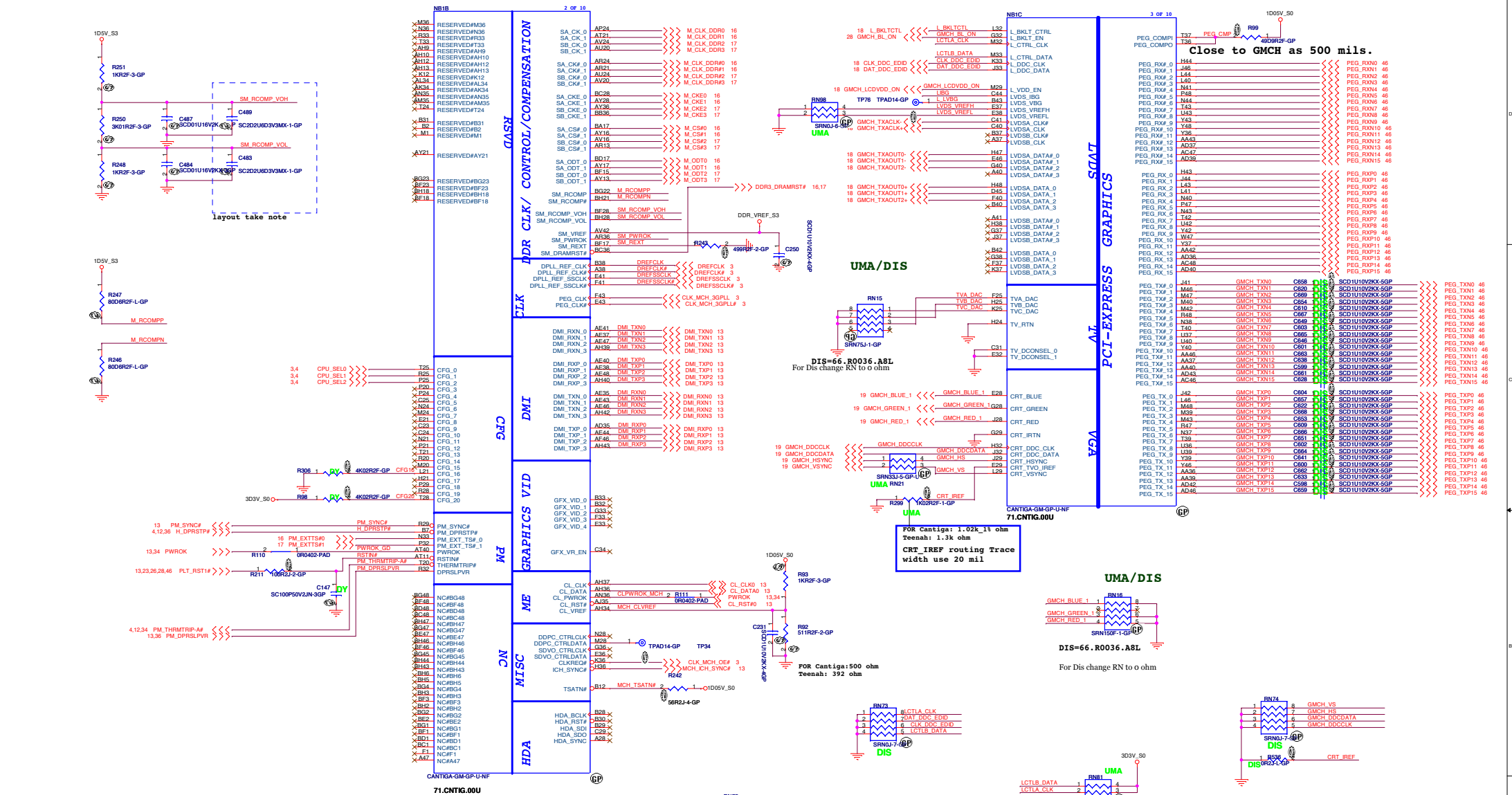
HOST



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Title		Cantiga (1 of 6) HOST	
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Pin Name Strap Description Configuration

CFG20

Digital DisplayPort (SDVO/DP/HDMI) Concurrent with PCIE

Low = Only digital DisplayPort (SDVO/DP/HDMI) or PCIE is operational (default)

High = Digital DisplayPort (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG port

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667MTS 2400mA
800MTS 3000mA

SC221MD3V/5VX-2GP
SC221MD3V/5VX-2GP

100V_S0_AKG
DIS

TP33 TPAD14-GP
TP32 TPAD14-GP

CANTIGA-GM-GP-U-NF
71.CNTIG.00U

VCC SM POWER

VCC GFX NCTF

VCC GFX

VCC BK LP

Ivcc_axg=8.7A

place near Cantiga

place near the Edge

Coupling CAP

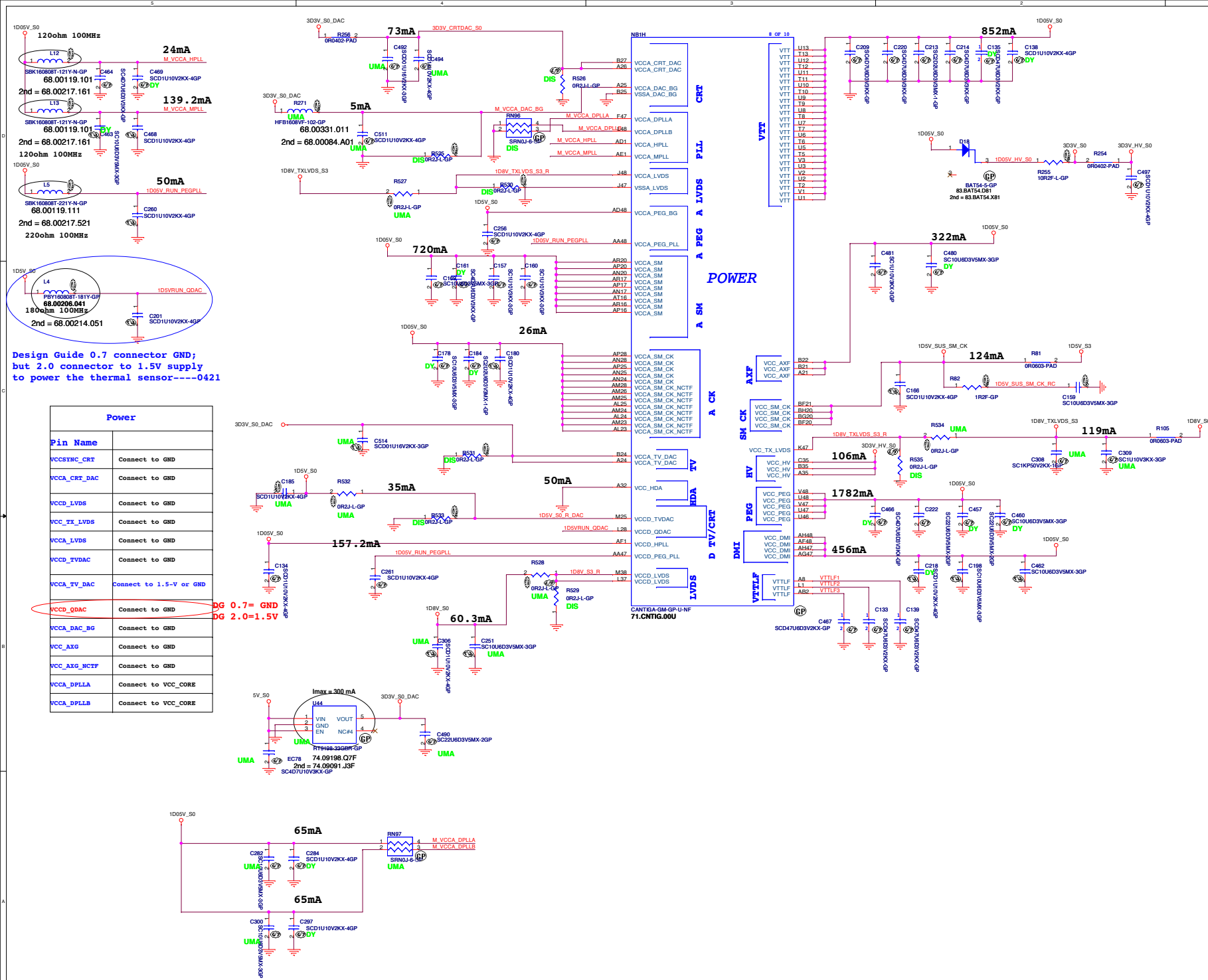
CANTIGA-GM-GP-U-NF
71.CNTIG.00U

VCC CORE

POWER

VCC NCTF

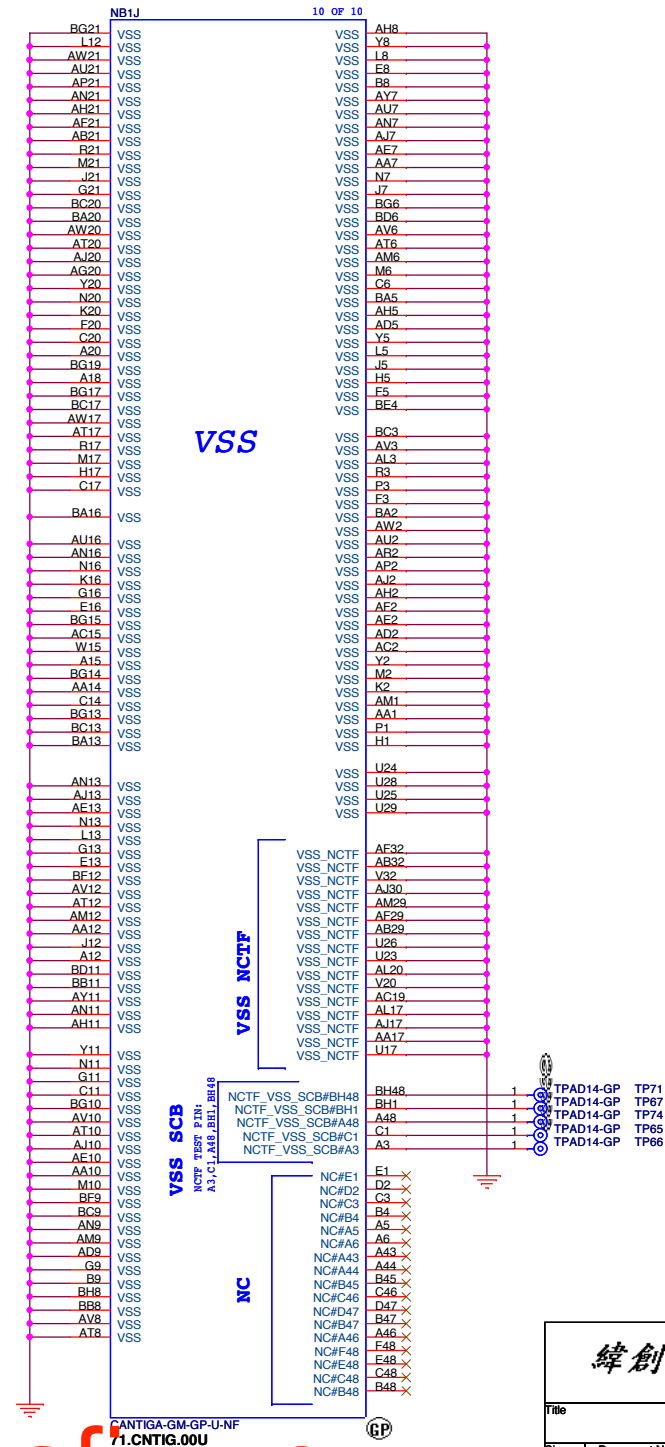
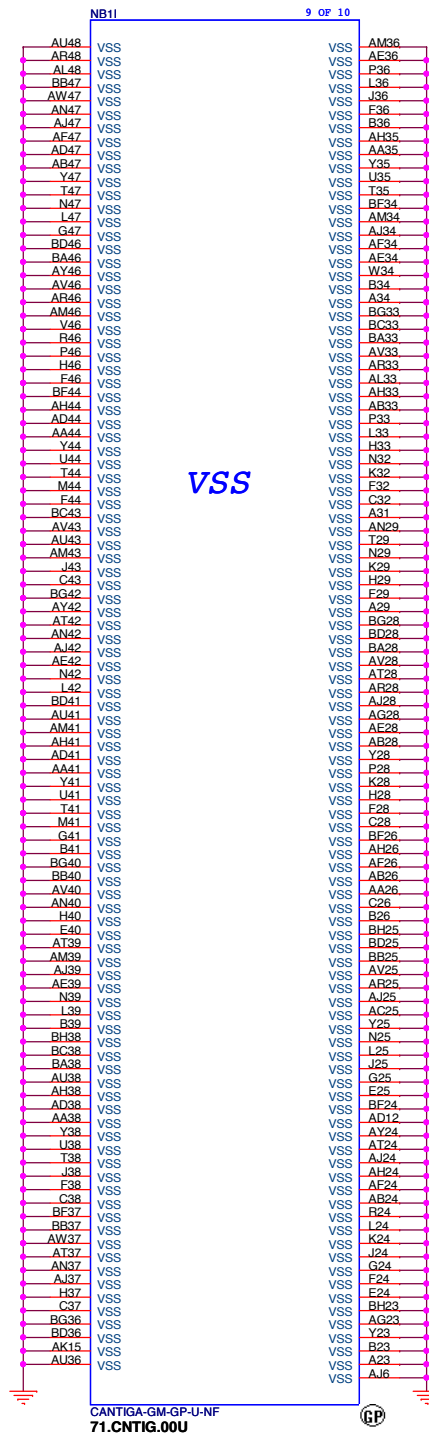
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Design Guide 0.7 connector GND;
but 2.0 connector to 1.5V supply
to power the thermal sensor----0421

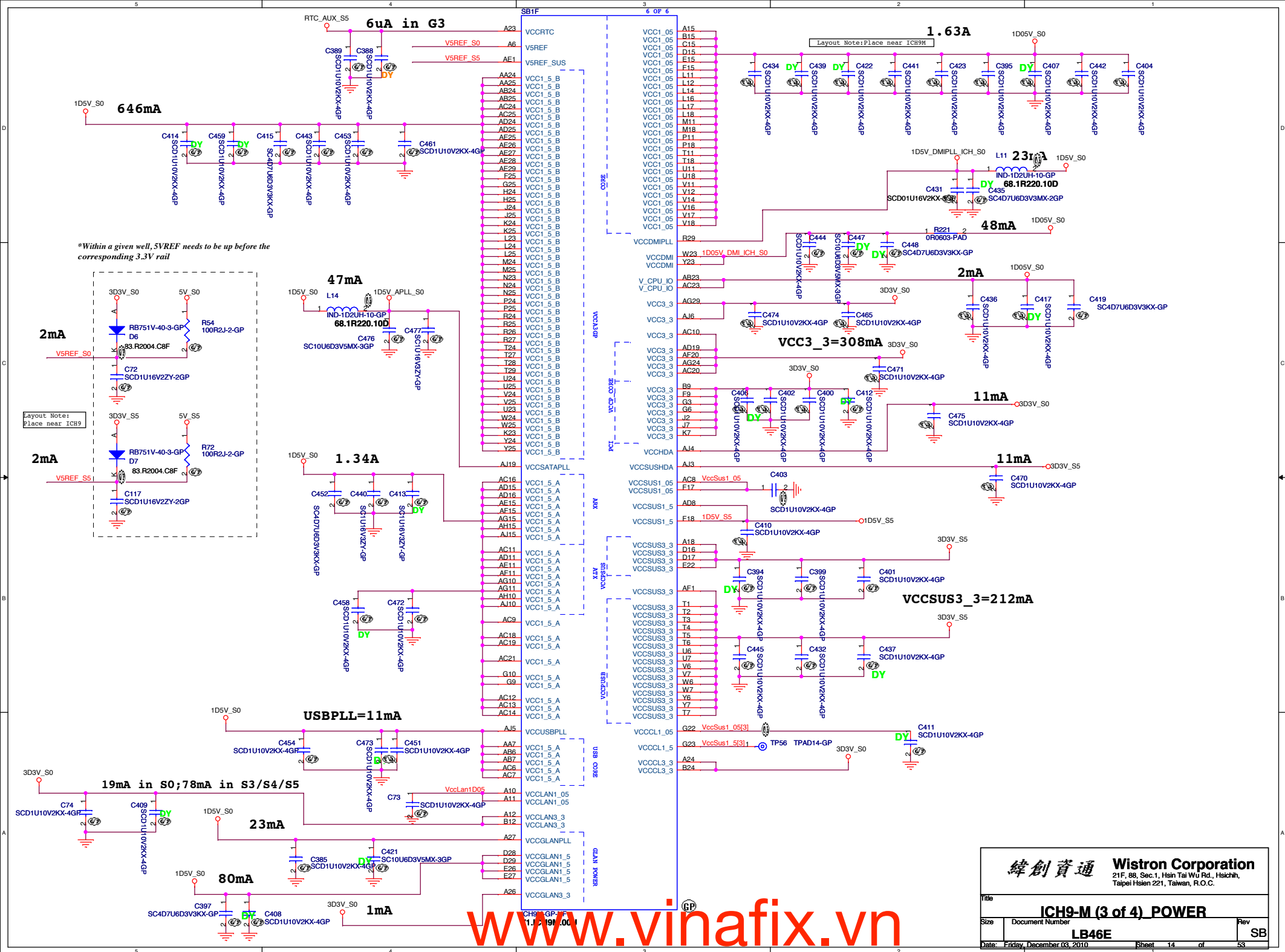
Power	
Pin Name	
VCCSYNC_CRT	Connect to GND
VCCA_CRT_DAC	Connect to GND
VCCD_LVDS	Connect to GND
VCC_TX_LVDS	Connect to GND
VCCA_LVDS	Connect to GND
VCCD_TV_DAC	Connect to GND
VCCA_TV_DAC	Connect to 1.5-V or GND
VCCD_QDAC	Connect to GND
VCCA_DAC_BG	Connect to GND
VCC_AXG	Connect to GND
VCC_AXG_NCTF	Connect to GND
VCCA_DPLLA	Connect to VCC_CORE
VCCA_DPLLB	Connect to VCC_CORE

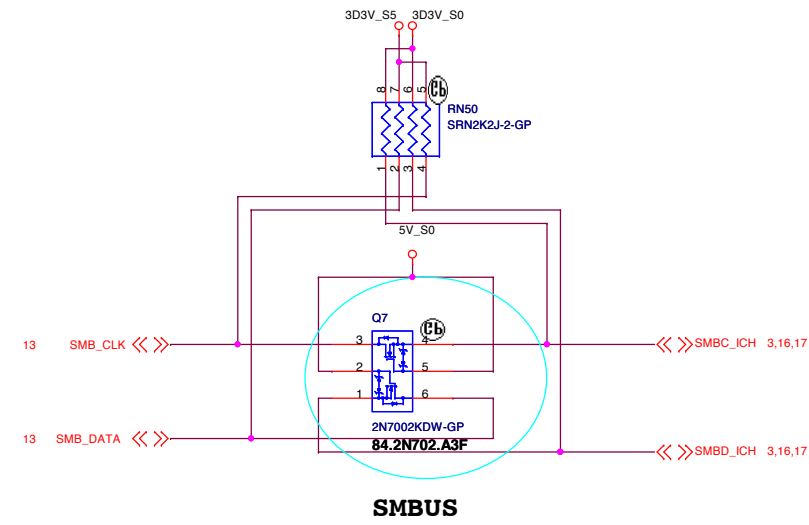
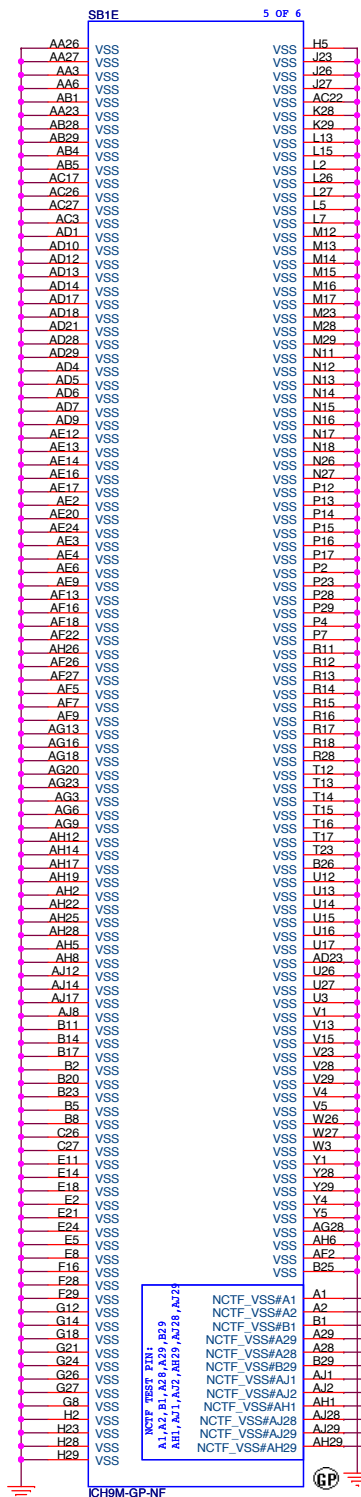
DG 0.7= GND
DG 2.0=1.5V





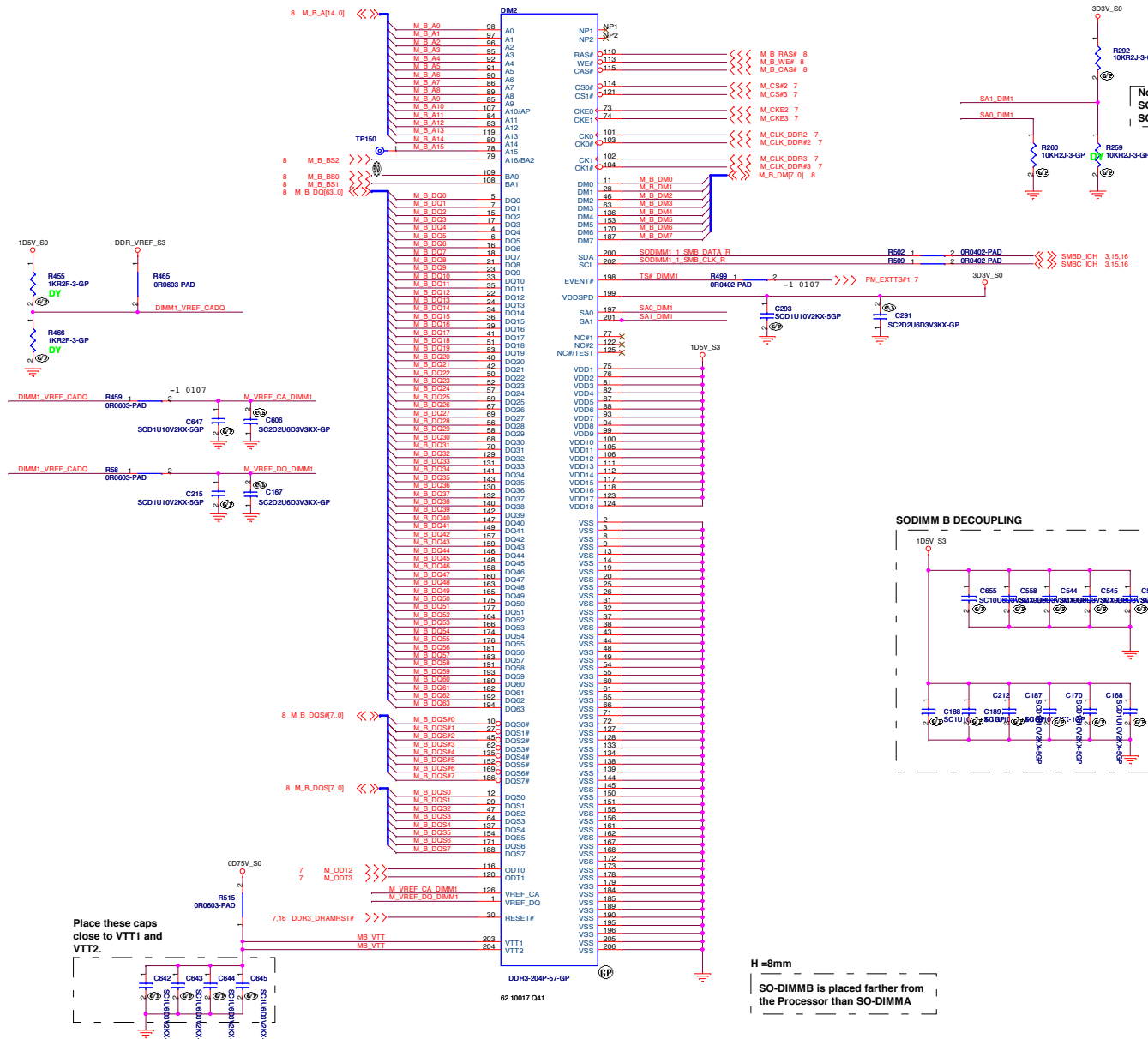




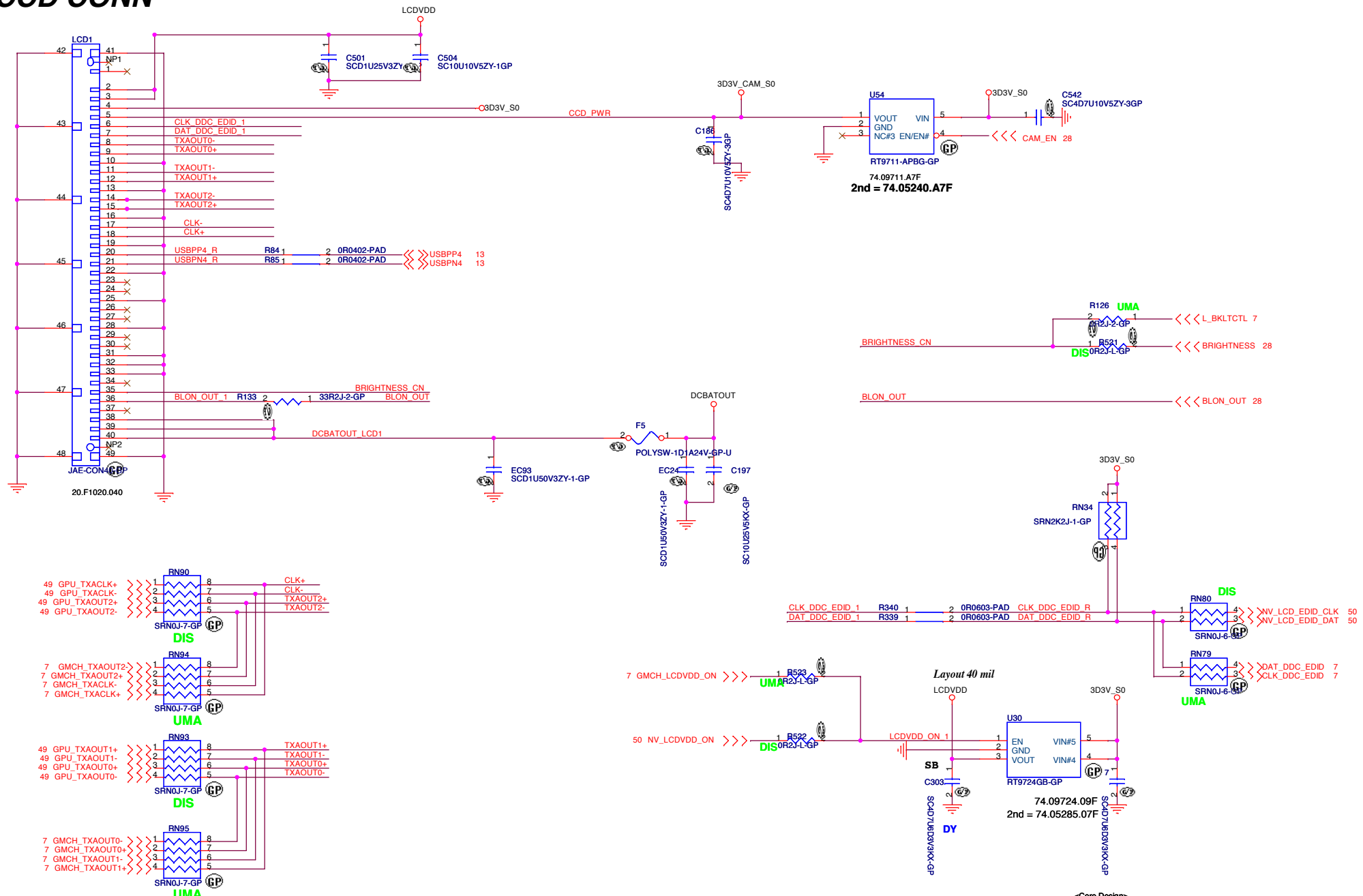


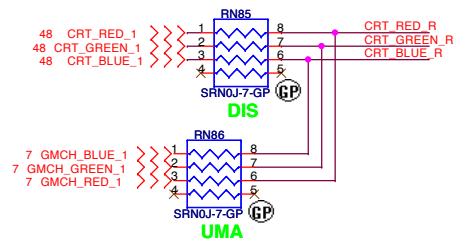
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2010/9/27 Changed



LCD/CCD CONN



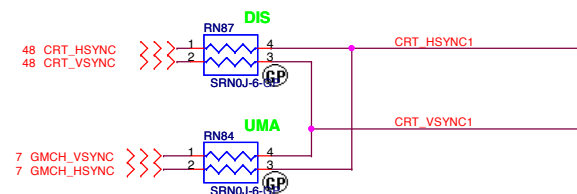


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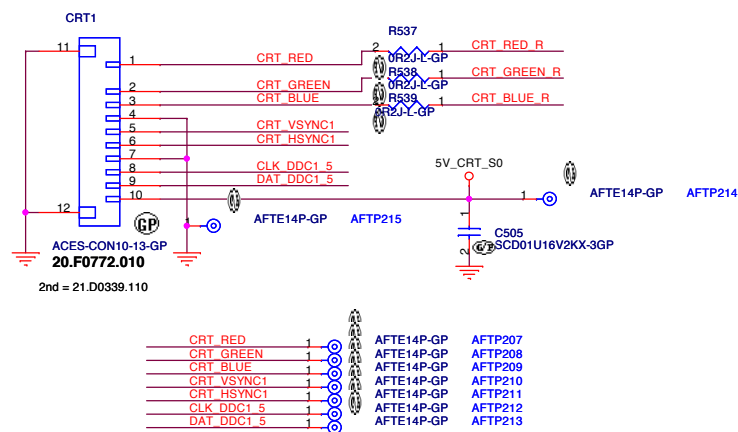
* Must be a ground return path between this ground and the ground on the VGA connector.

Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

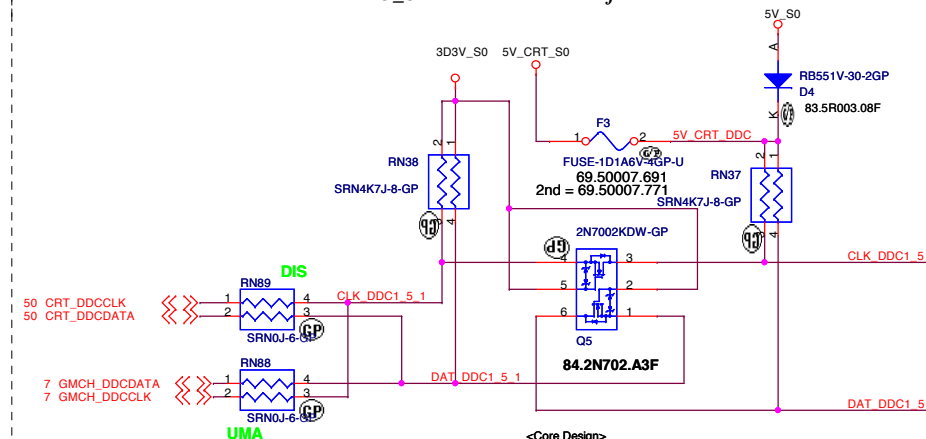
Hsync & Vsync level shift



CRT I/F & CONNECTOR



DDC_CLK & DATA level shift



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CRT Connector

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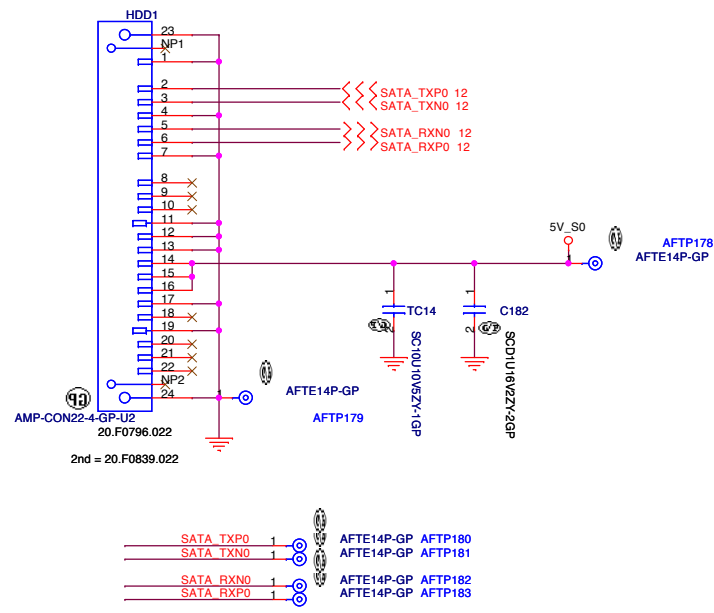
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SB

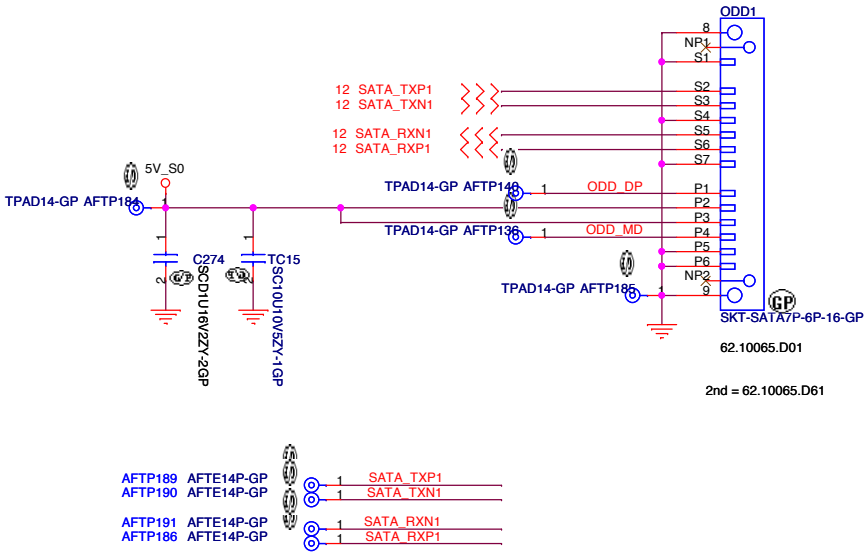
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SATA Connector

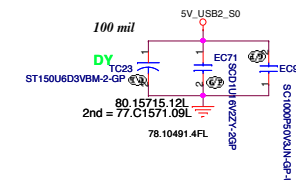
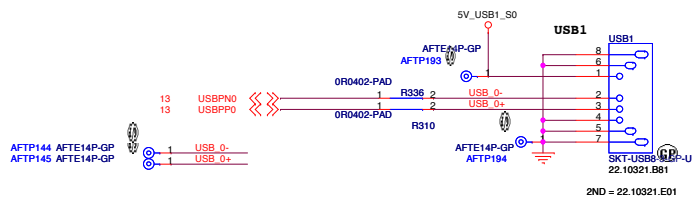
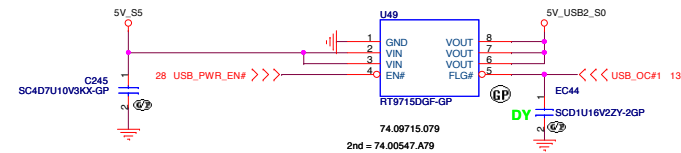
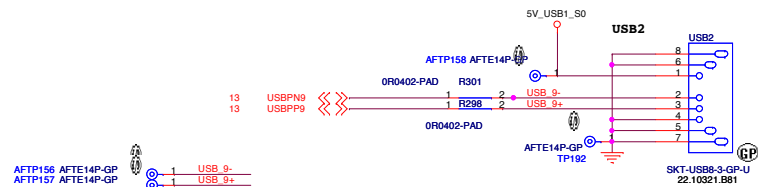


SATA ODD Connector

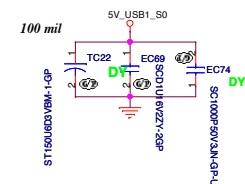
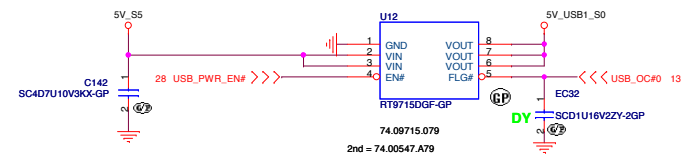
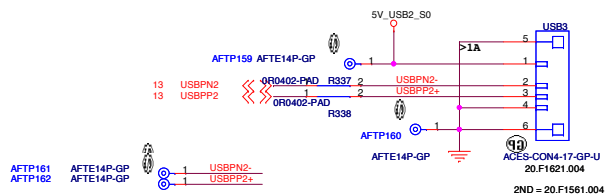


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Size	Document Number		Rev
	LB46E		SB
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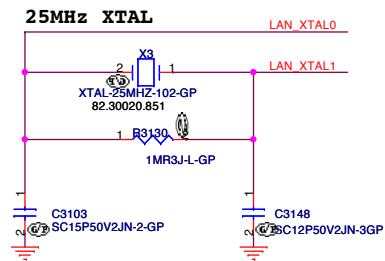
Connect to USB BD



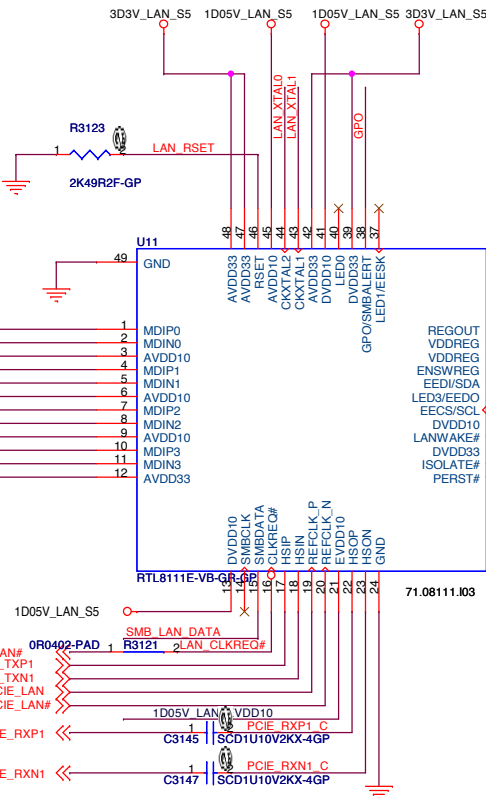
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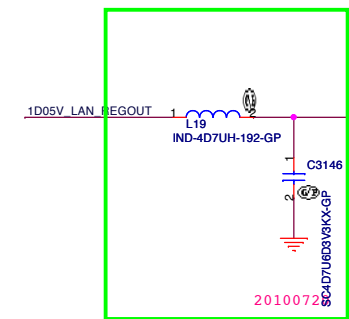
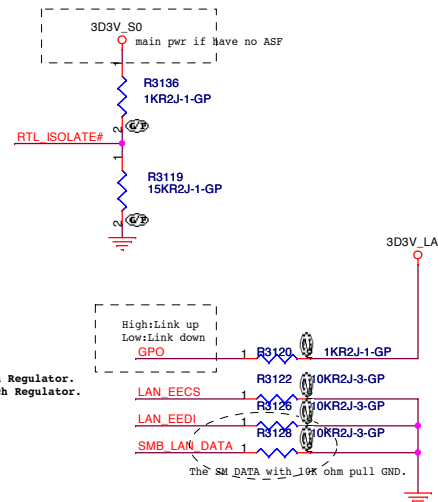
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Size	Document Number	LB46E	Rev
Date	Monday, December 27, 2010	Sheet	22 of 53



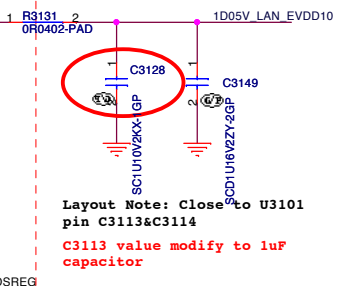
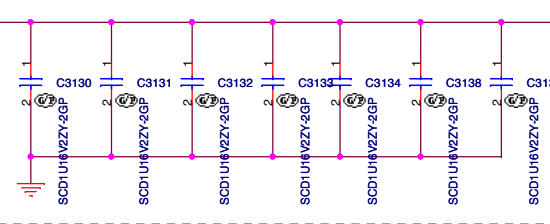
Pin-XTAL2 is External Clock Input Pin.
R3121 is need when using external clock source.



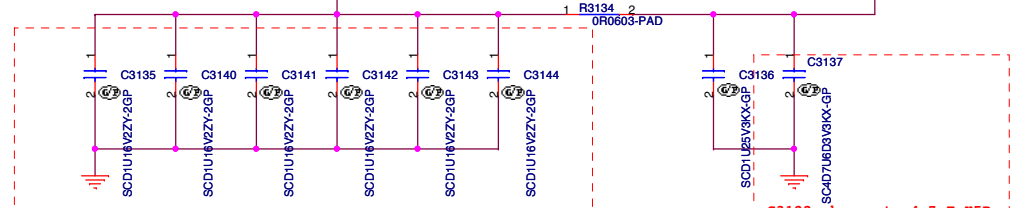
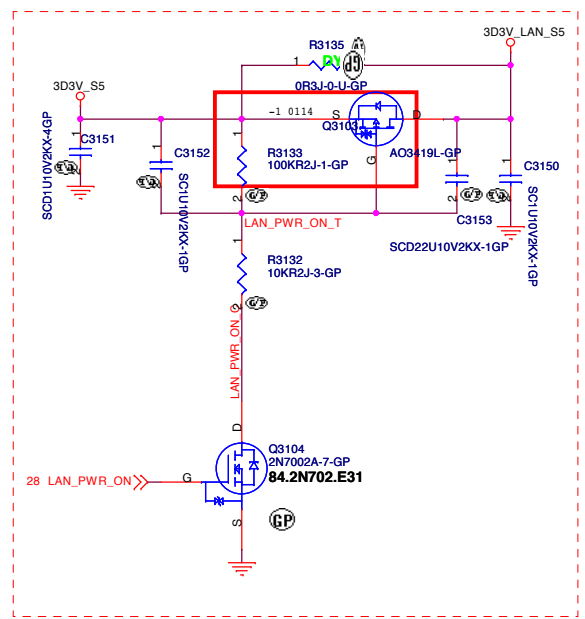
Make sure PCIE_Wake# & PCIE_CLK_LAN_RQ1# connected to 10K resistor pull high close to PCH side



Layout Note: Close to U3101 pin C3106 ~ C3112



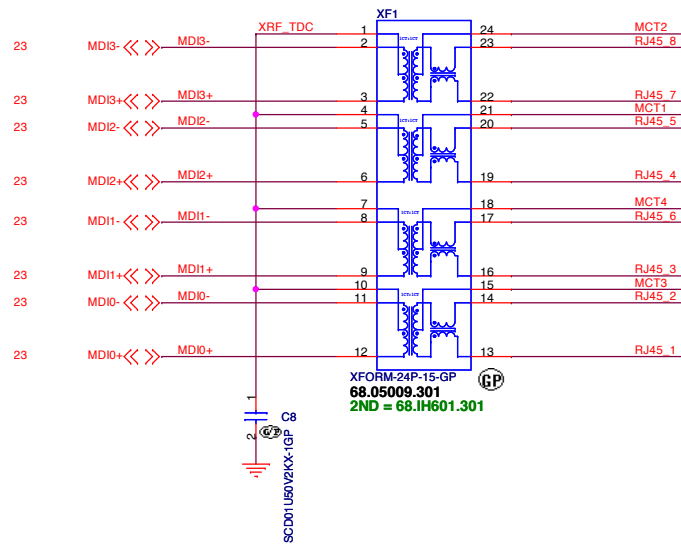
Layout Note: Close to U3101 pin C3113&C3114
C3113 value modify to 1uF capacitor



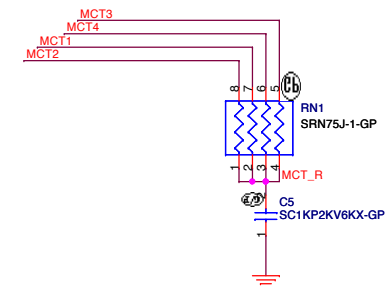
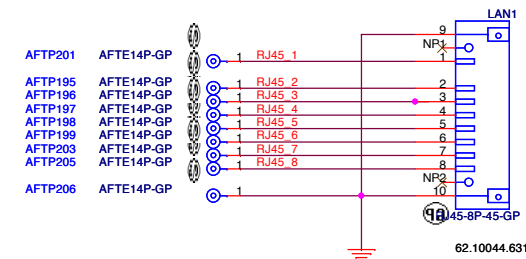
Layout Note: Close to U3101 pin C3115 ~ C3120

C3122 change to 4.7uF X5R type capacitor

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



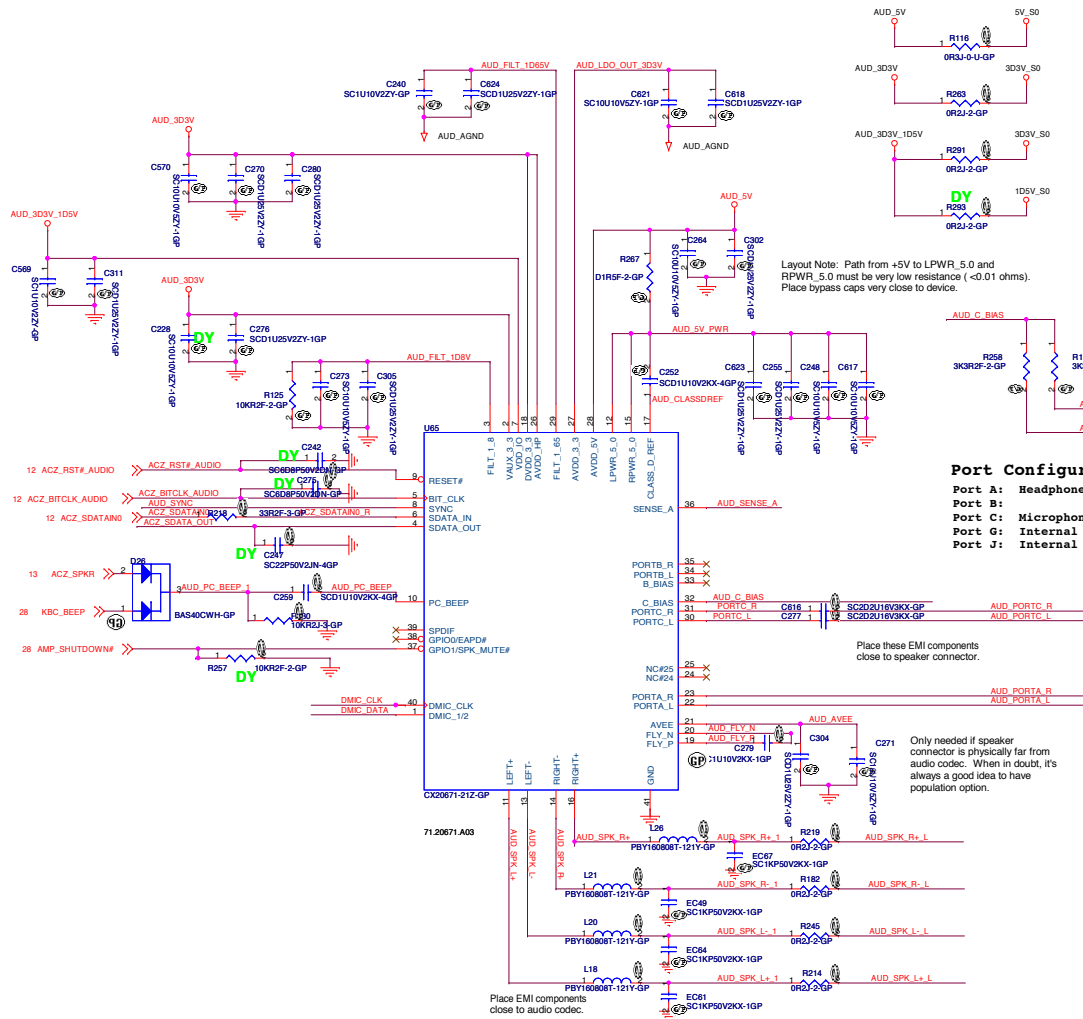
LAN Connector



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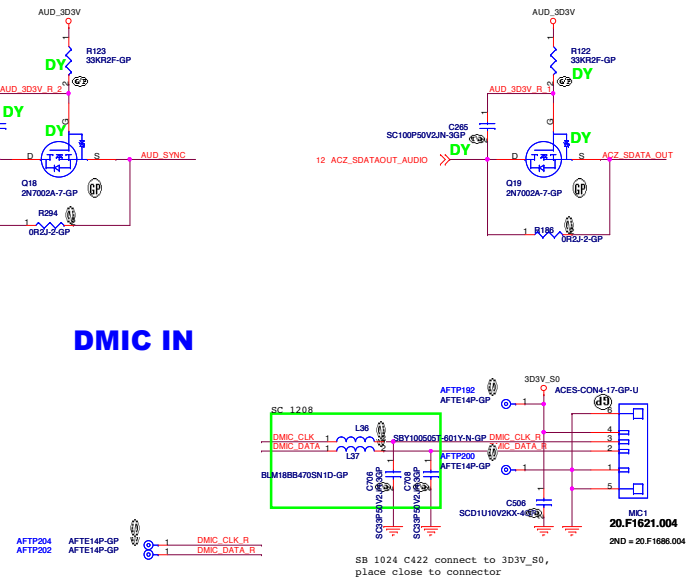
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Size	Document Number	Rev		SB
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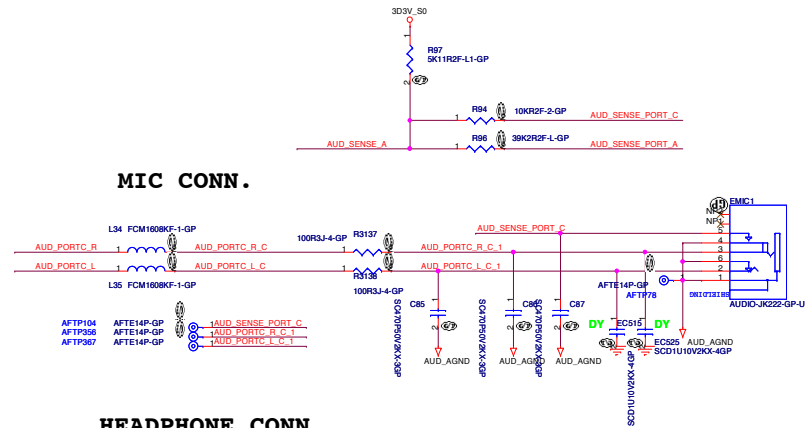


Port Configuration
 Port A: Headphone jack
 Port B: Headphone jack
 Port C: Microphone jack
 Port G: Internal stereo speakers
 Port J: Internal stereo digital mic

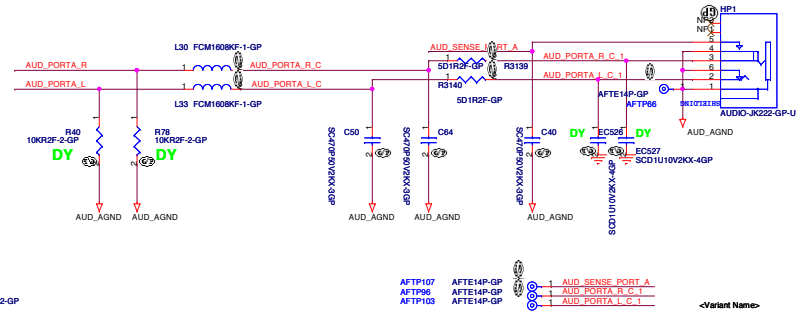
DMIC IN



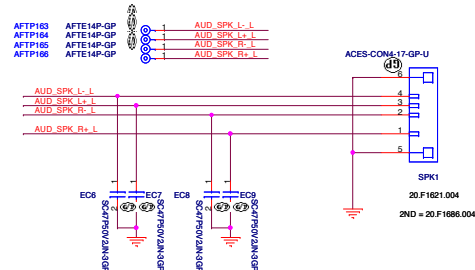
MIC CONN.



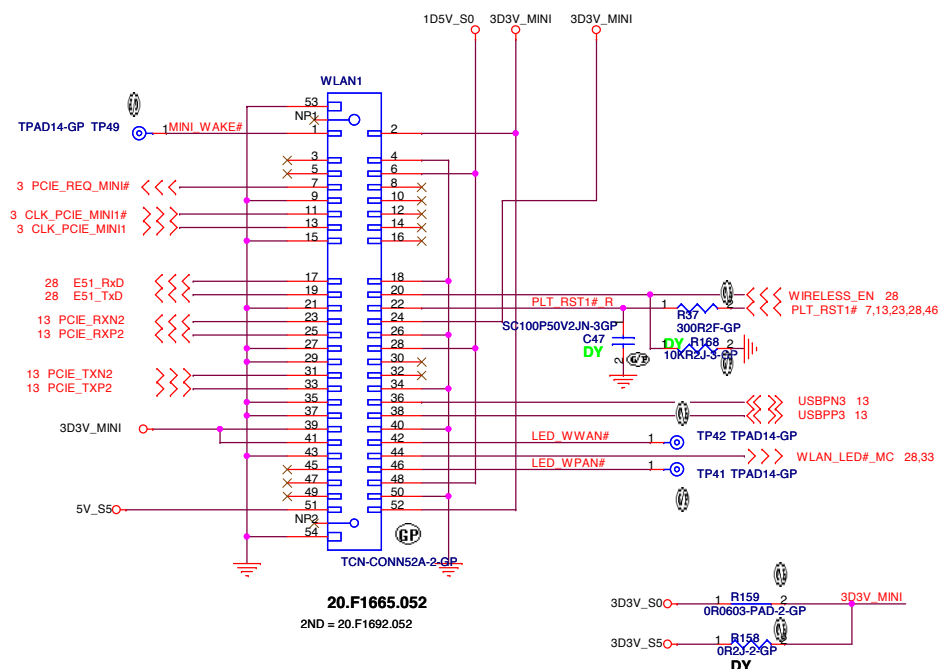
HEADPHONE CONN.



Internal Speaker



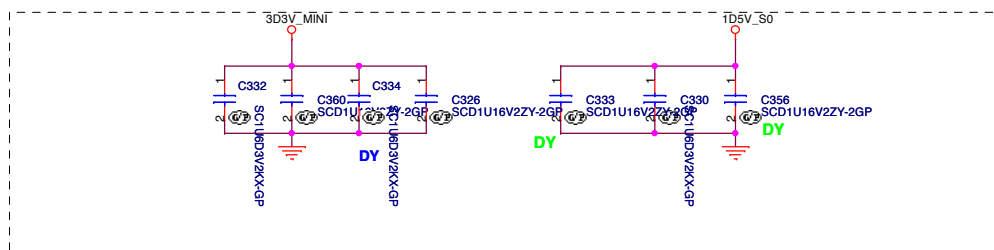
Mini Card Connector(WLAN)



20.F1665.052

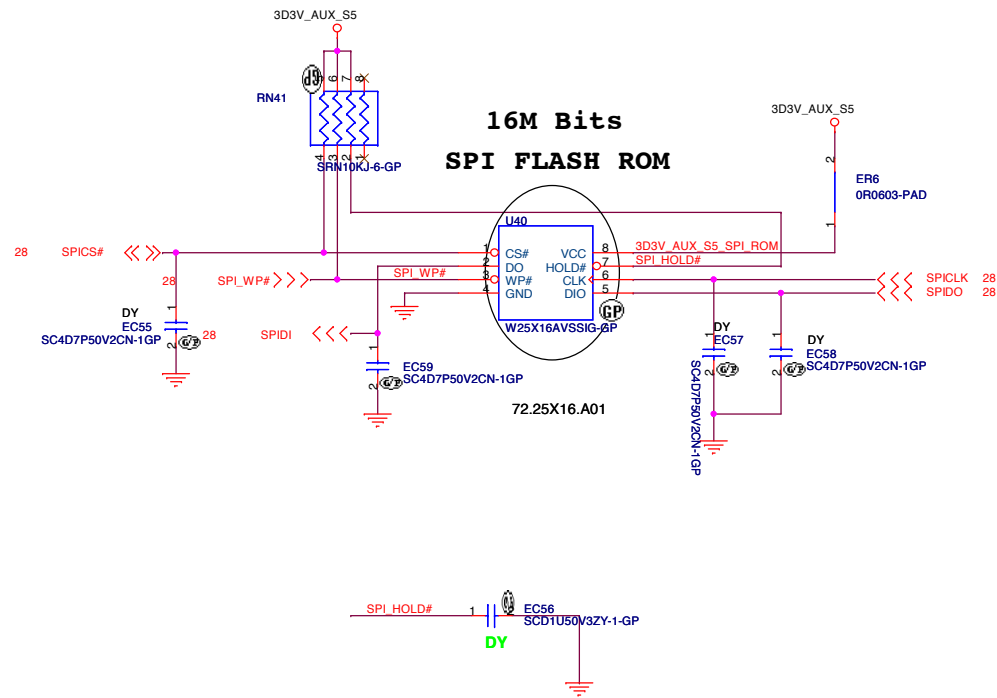
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Place near MINIC1



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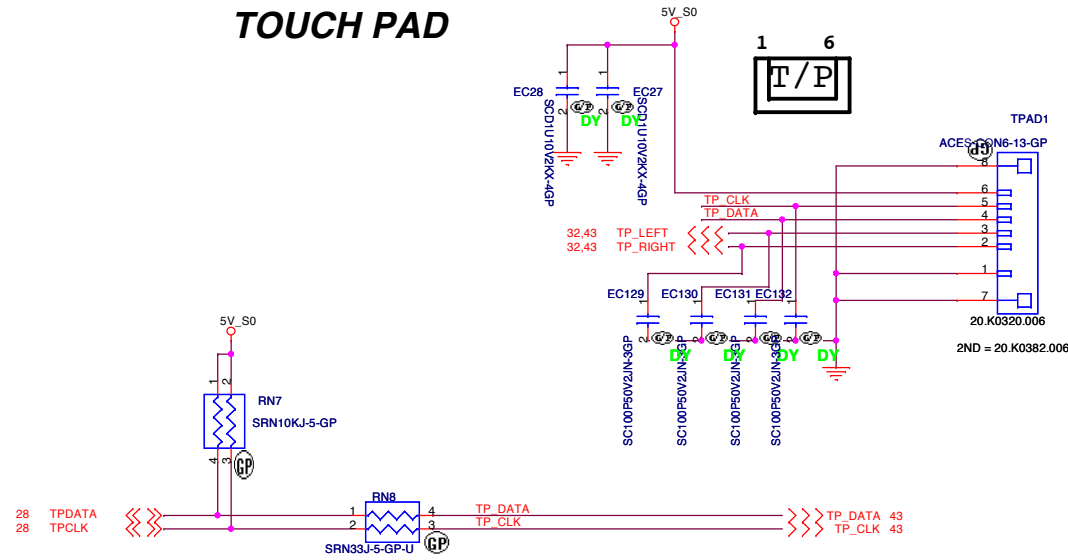
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
MINI CARD			
Size	Document Number		Rev
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Title		BIOS	
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TOUCH PAD



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Title

Touch pad

Size

Document Number

LB46E

Rev

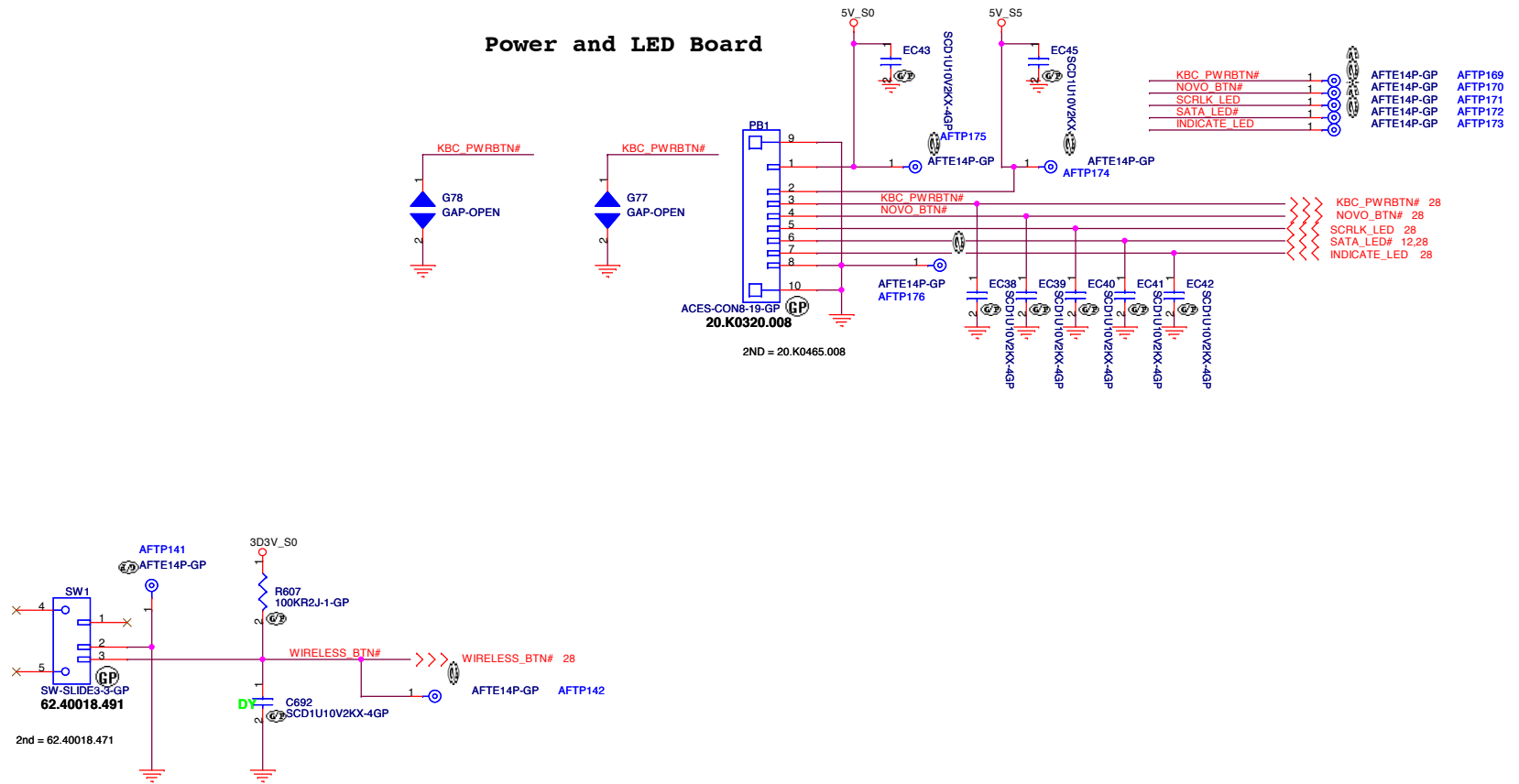
SB

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Power and LED Board



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Title

Power Board

Size

Document Number

LB46E

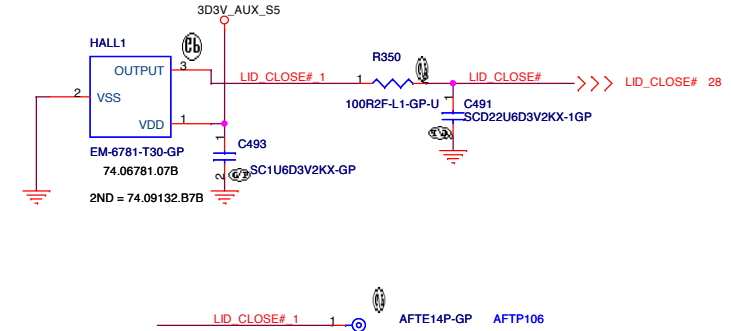
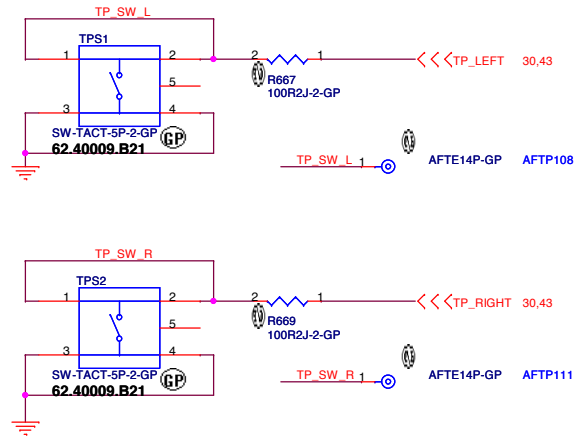
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Date: Monday, December 27, 2010

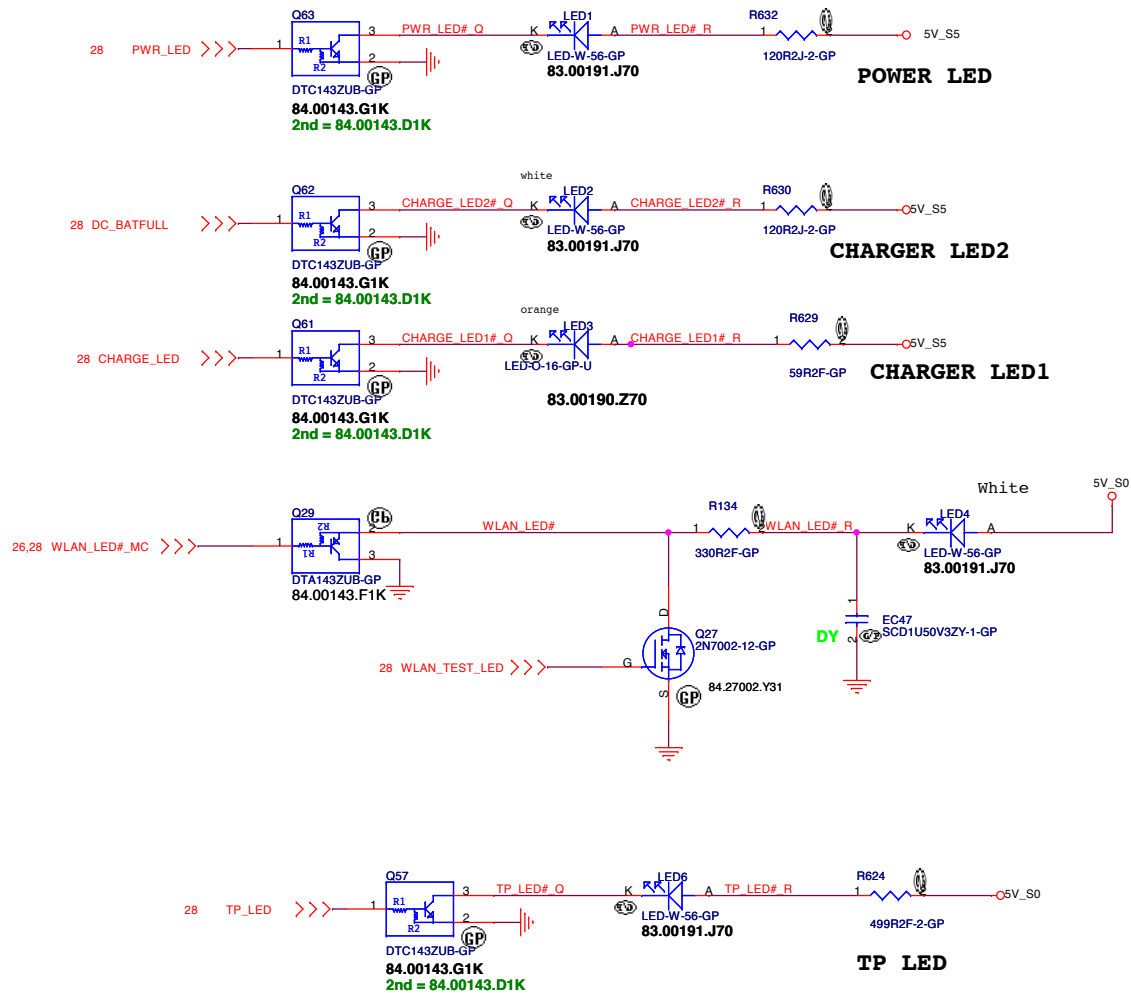
Sheet 31 of 53

Cover Up Switch



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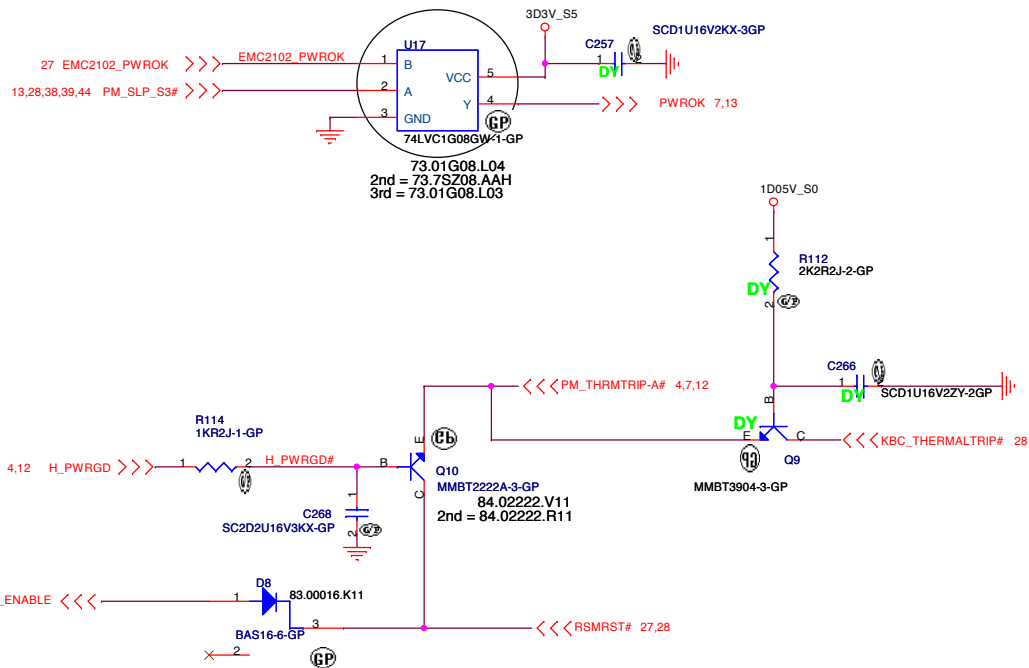
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		Title	
Size		Document Number	
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Title		SWITCHS	
Size		Document Number	
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Title		SWITCHS	
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LED			
Size	Document Number	Rev	
	LB46E	SB	
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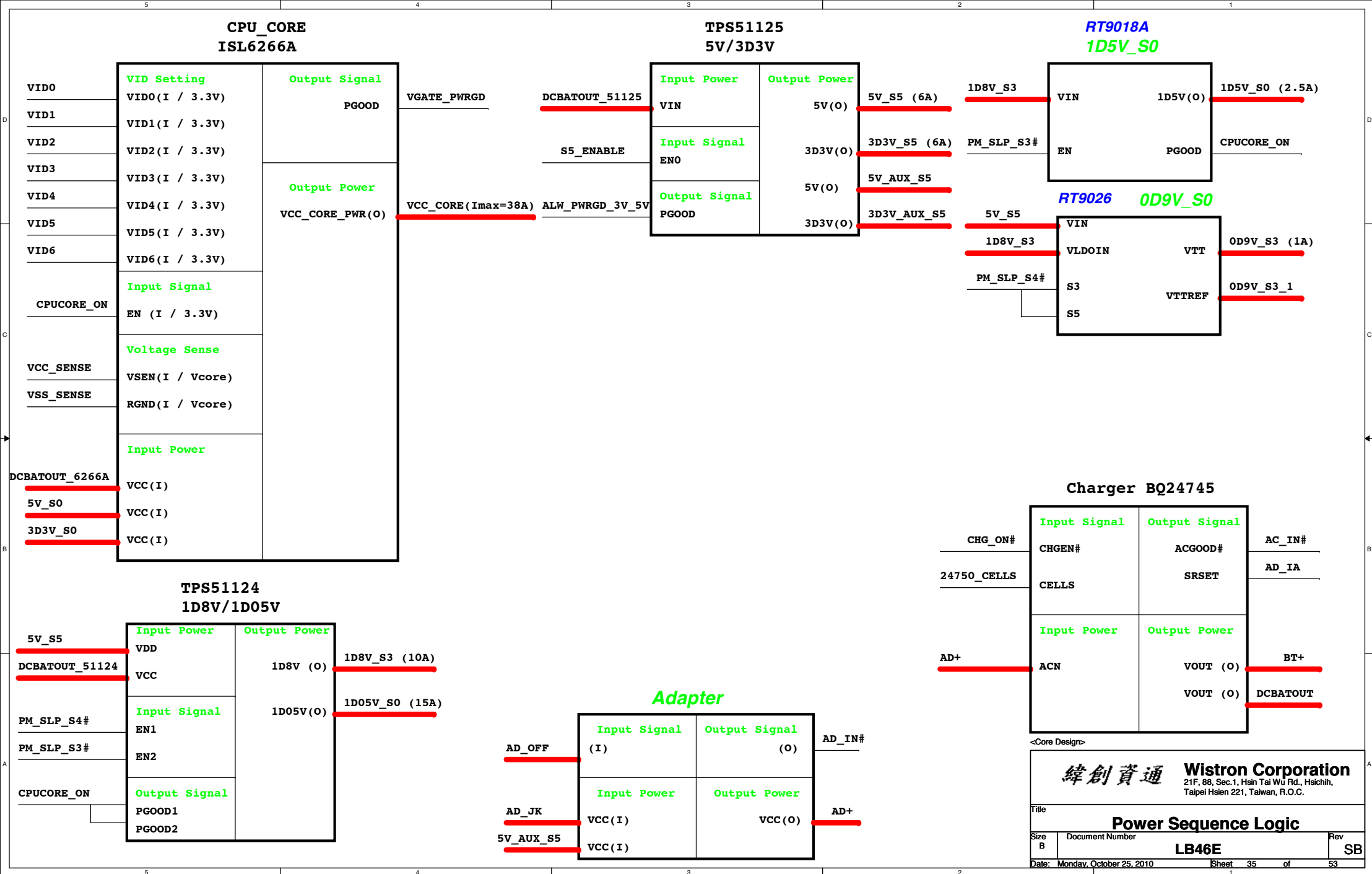
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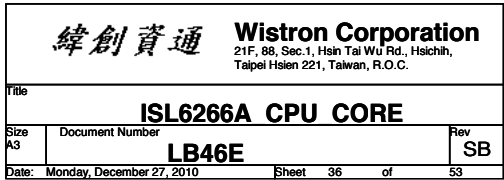


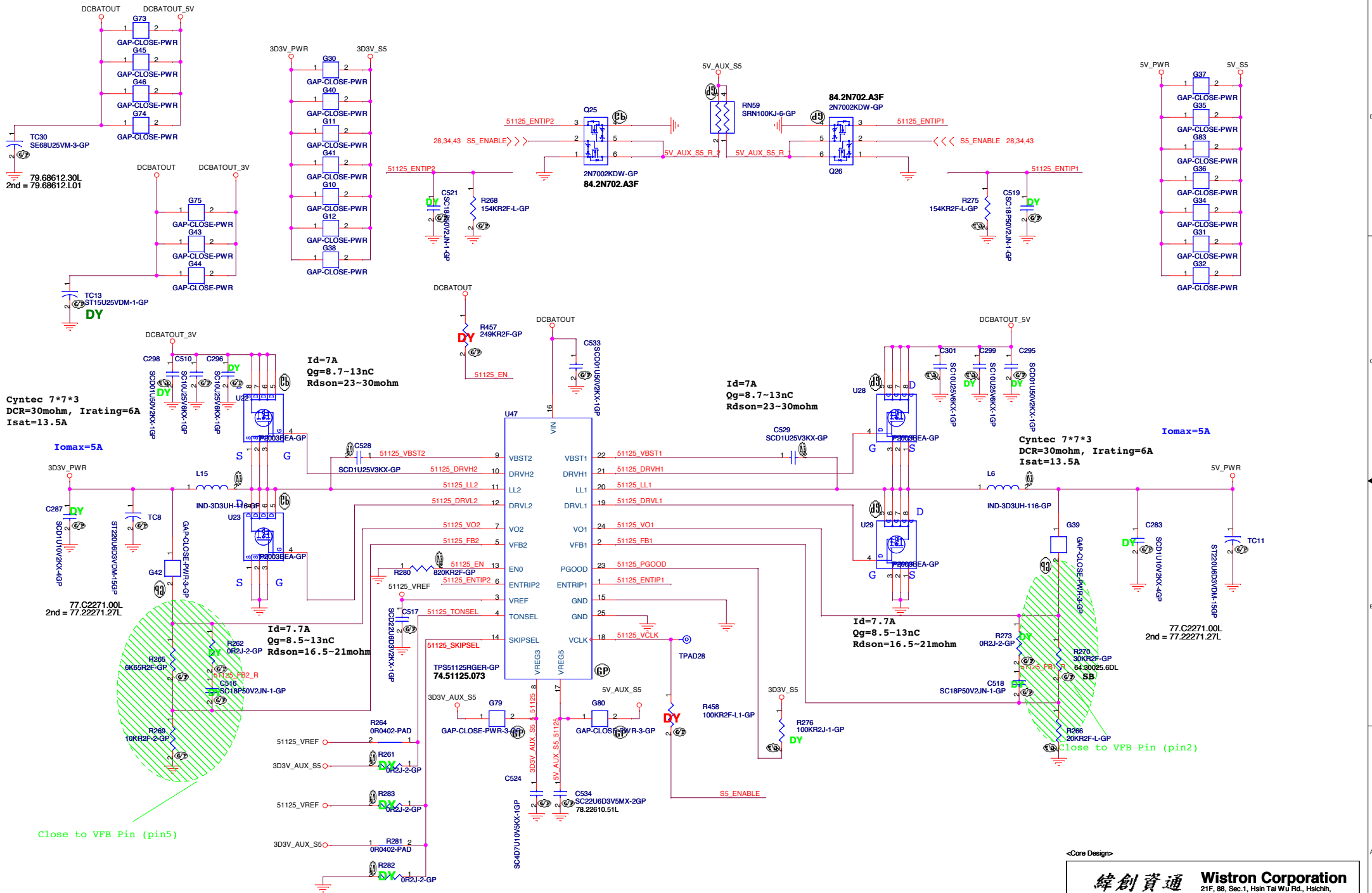
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Size	Document Number	Rev
	LB46E	SE

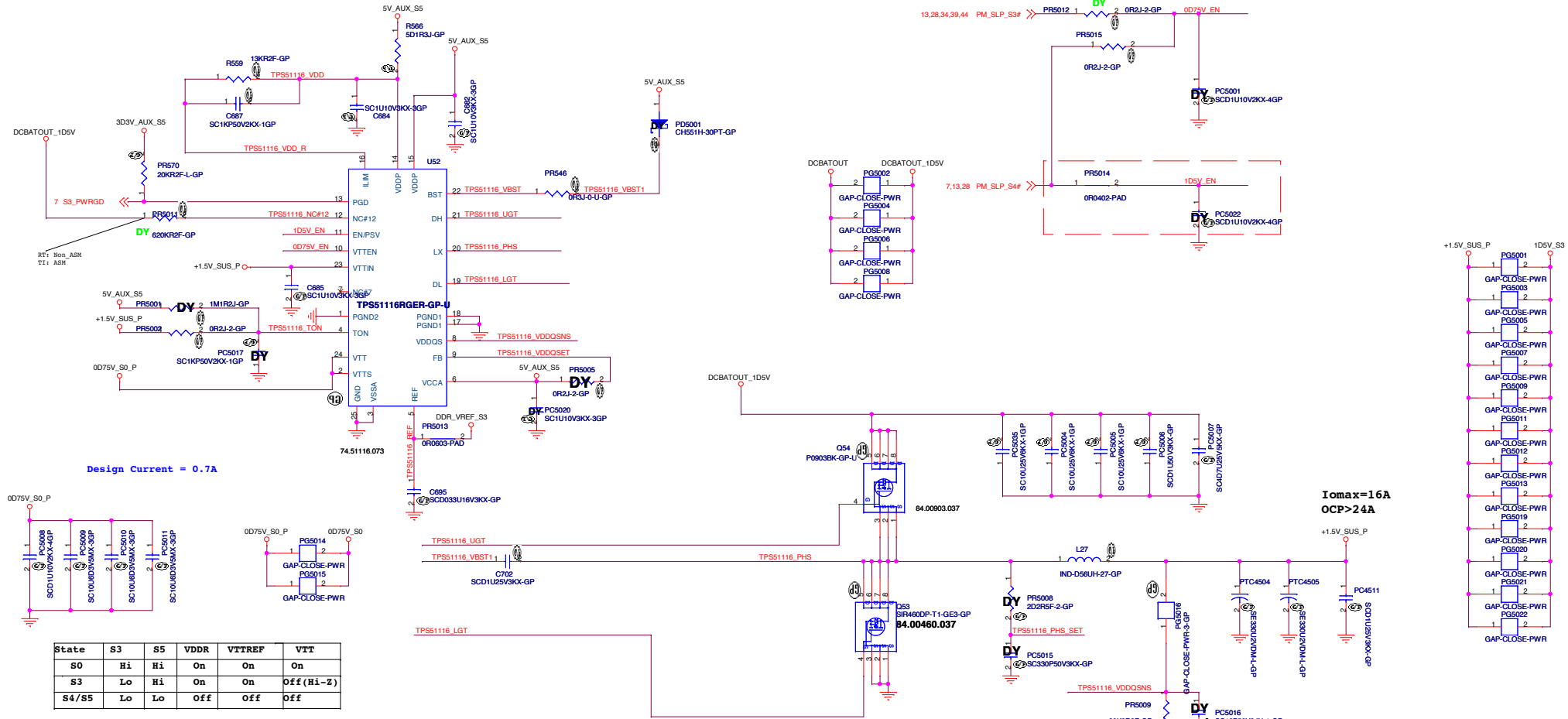
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SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
 O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L0
 H/S: S1S406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
 L/S: S1S402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037
 Switching freq-->400KHz

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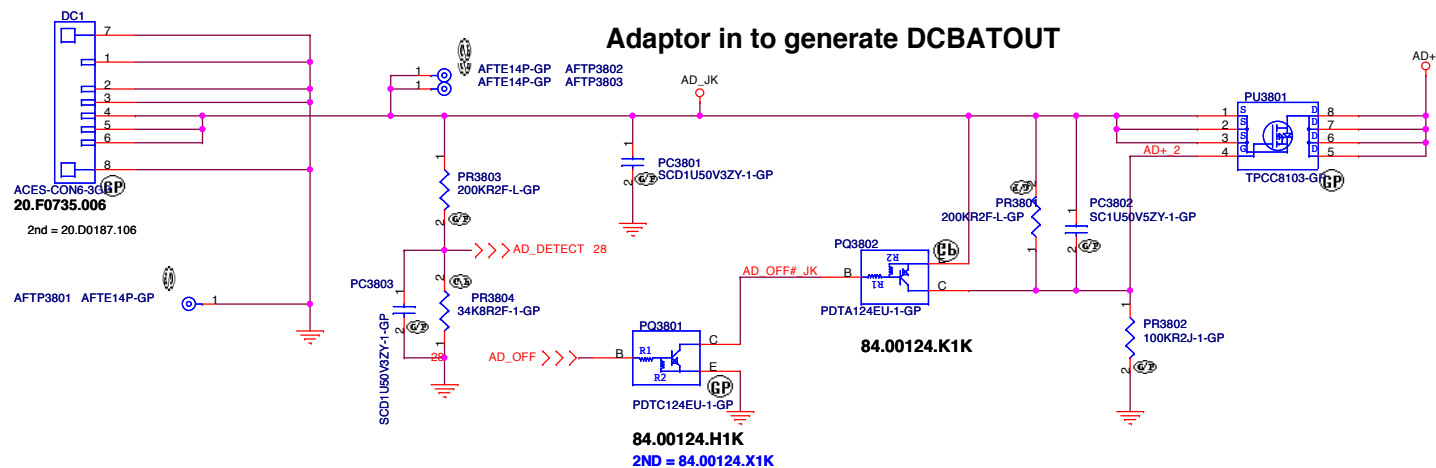
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51116 +1.5V S3**

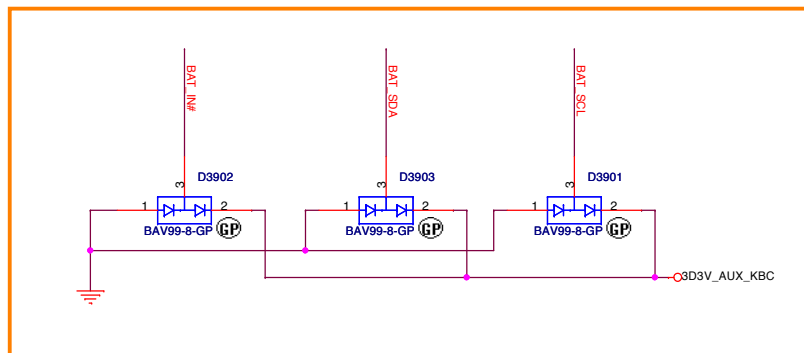
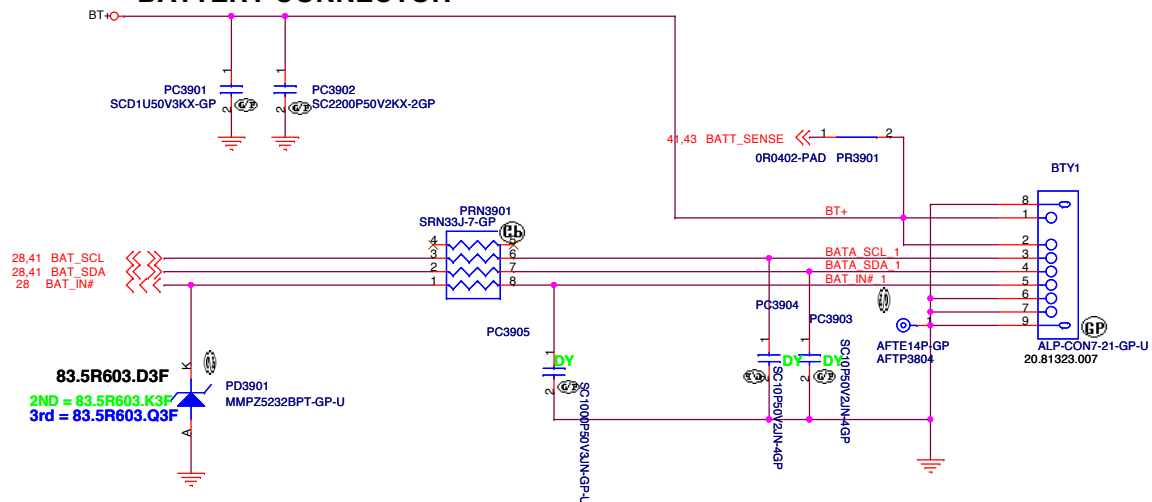
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Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Title

AD/BATT CONN

Size

Document Number

LB46E


Rev

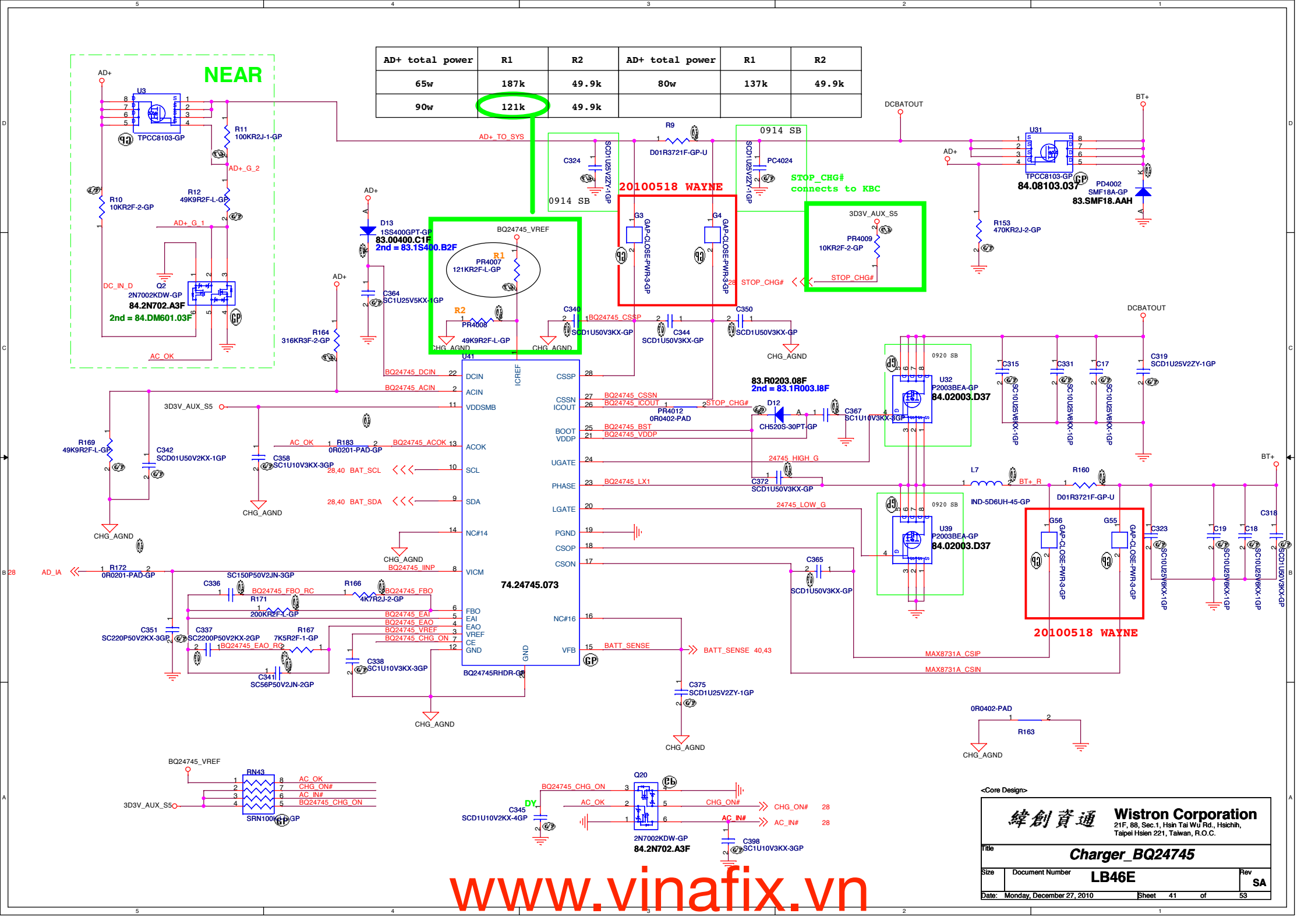
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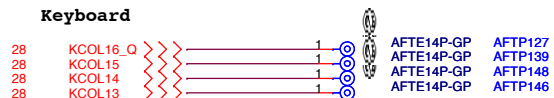
Date: Monday, December 27, 2010

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Title			
Charger_BQ24745			
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Check test point



Test Point locate near DIMM Door where can be tested



FAN

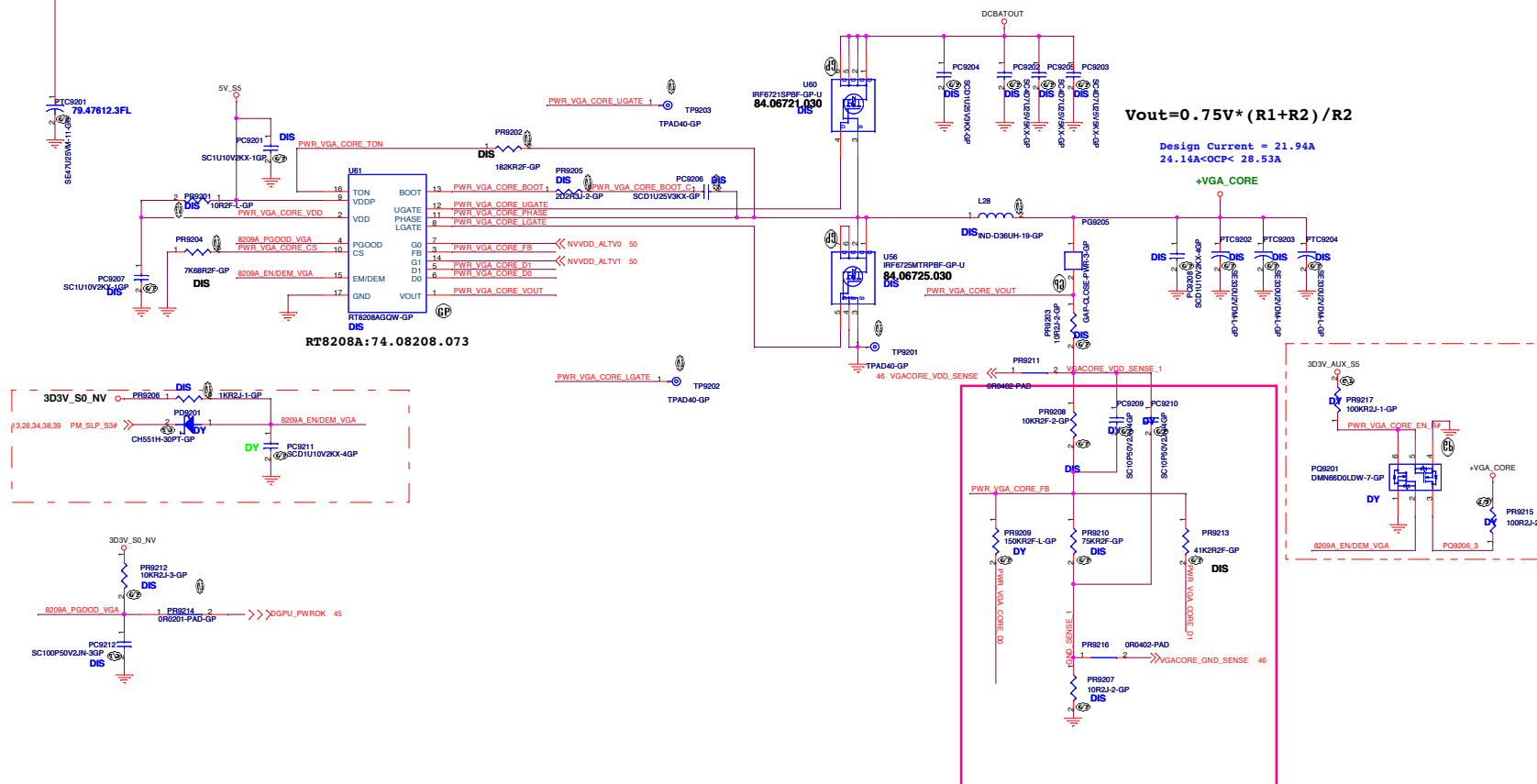


Cover Switch



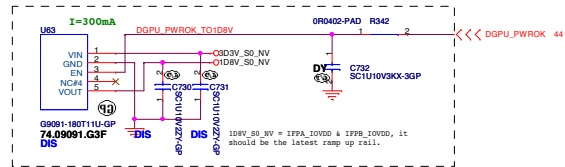
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Title			
AFTE test point			
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SSID = PWR.Plane.Regulator_GFX

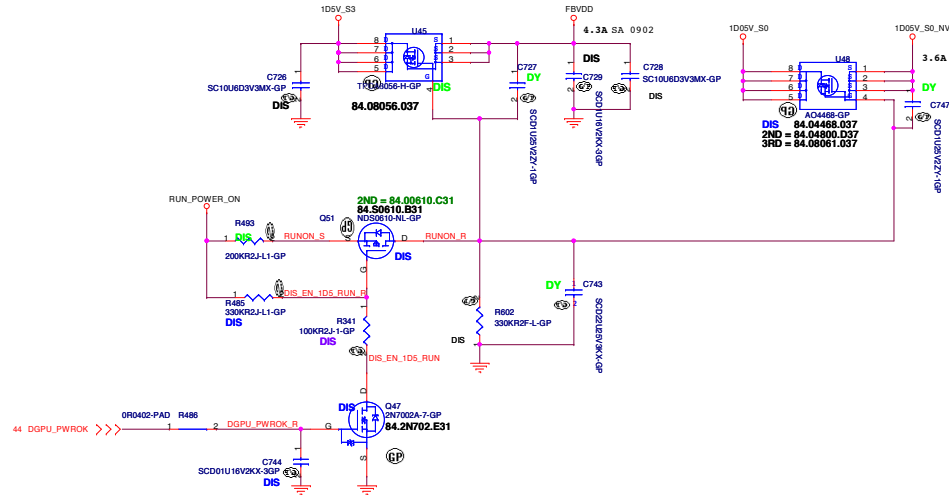
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Del +3VS to 1.8V Transfer for OP 0119 +3VS to 1.8V Transfer



+1.5V to FBVDD Transfer

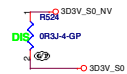
+1.05V to +1.05V_NV Transfer



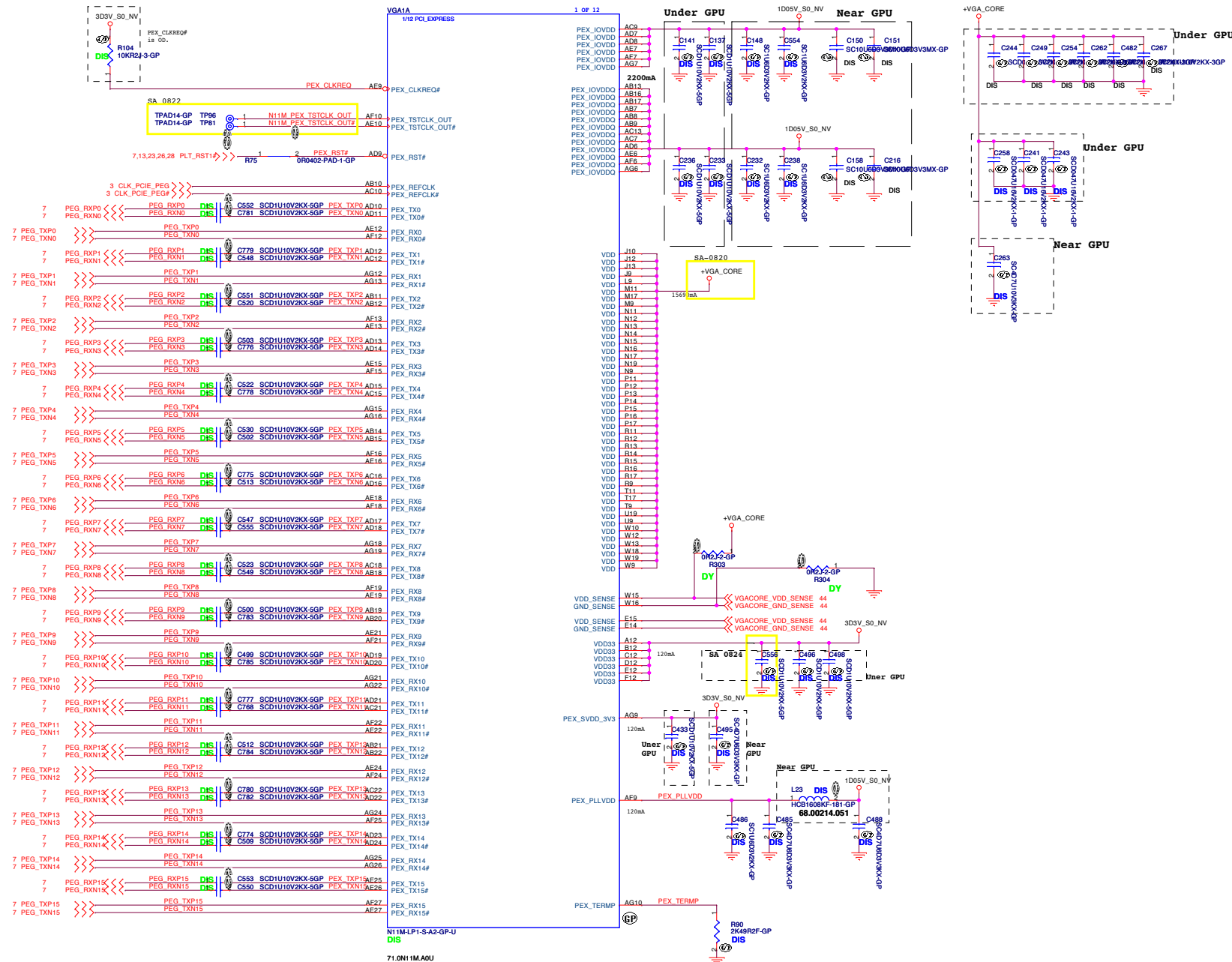
+3VS to 3.3V_DELAY Transfer

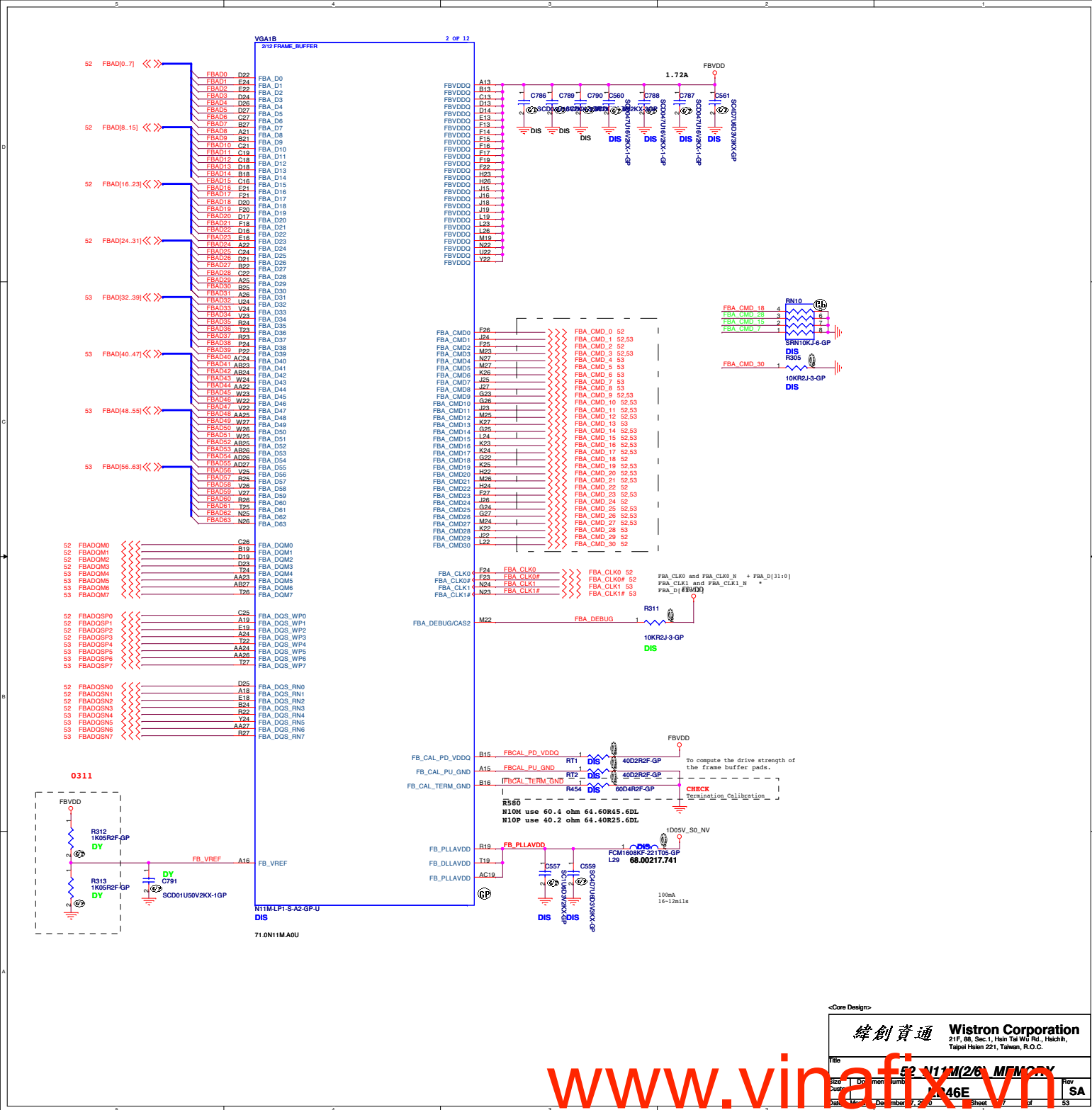
3.3v (580mA)

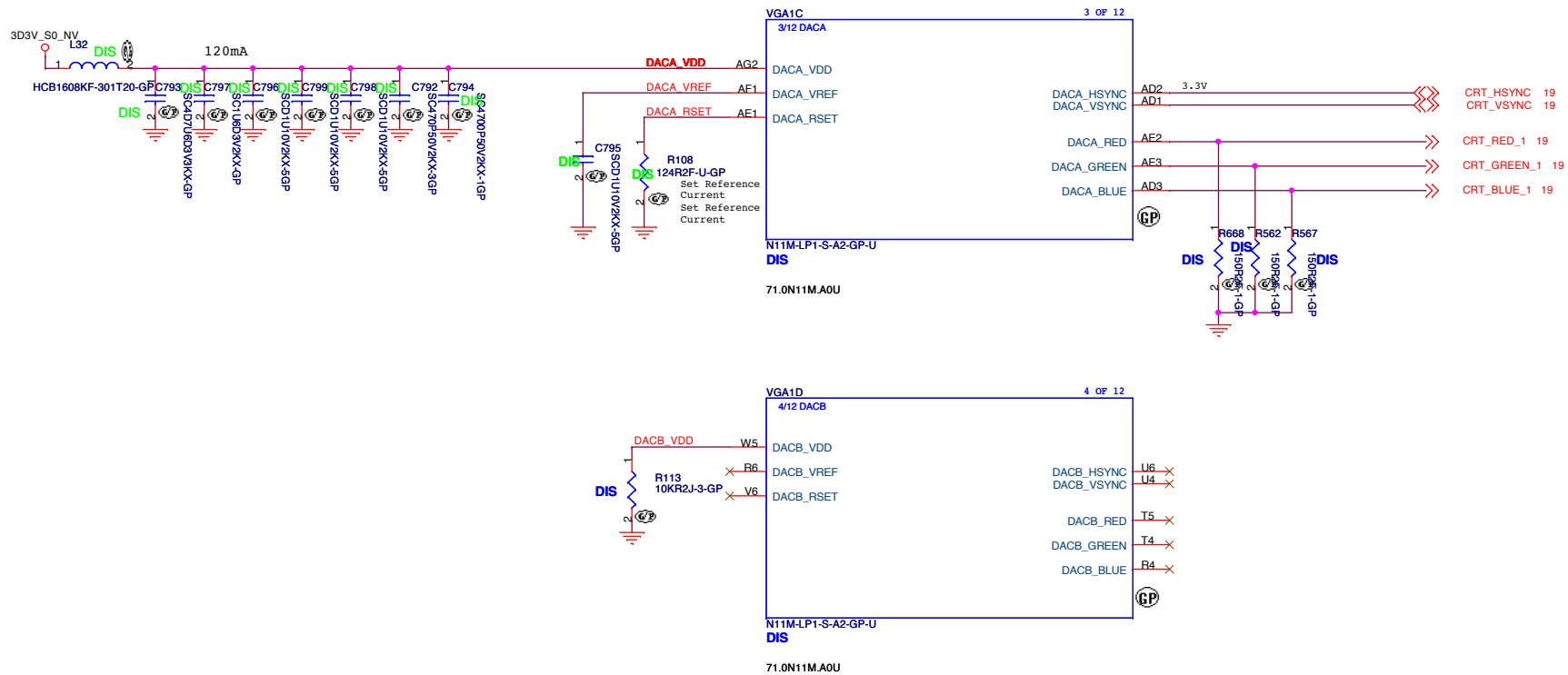
VDDR3discharge CKT



71.0N11M.C1U



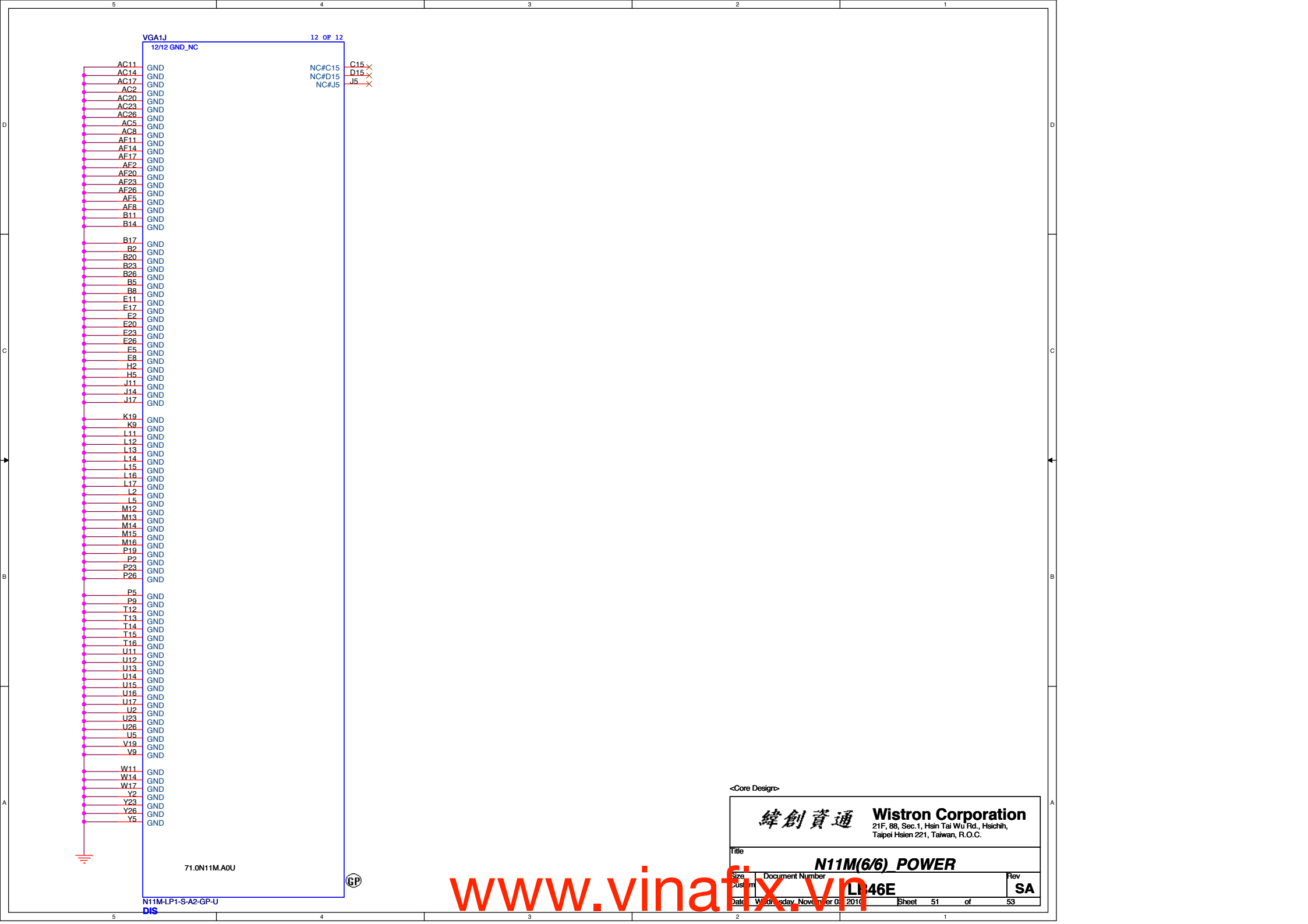


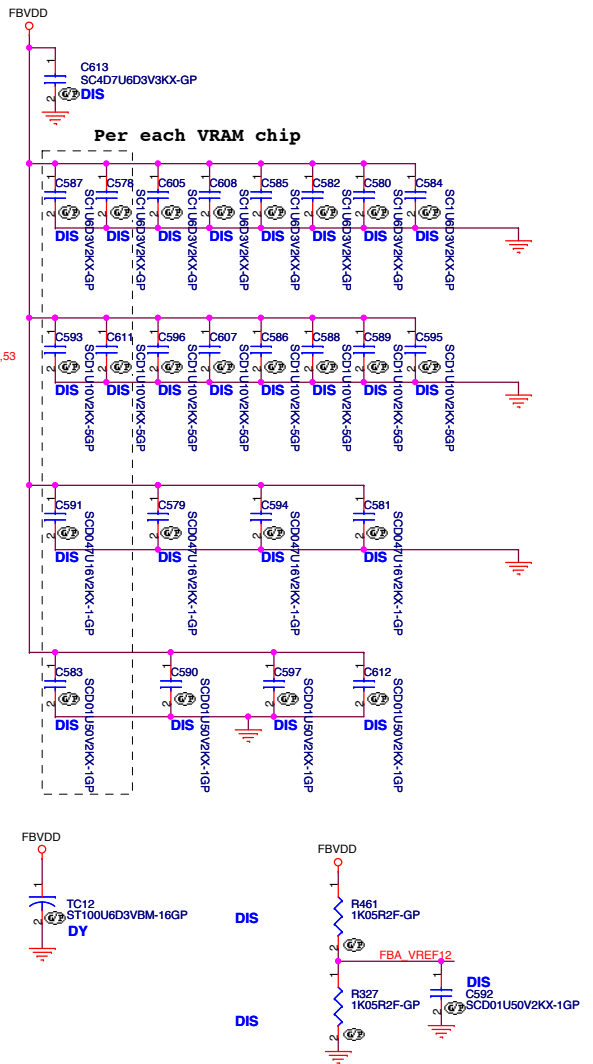
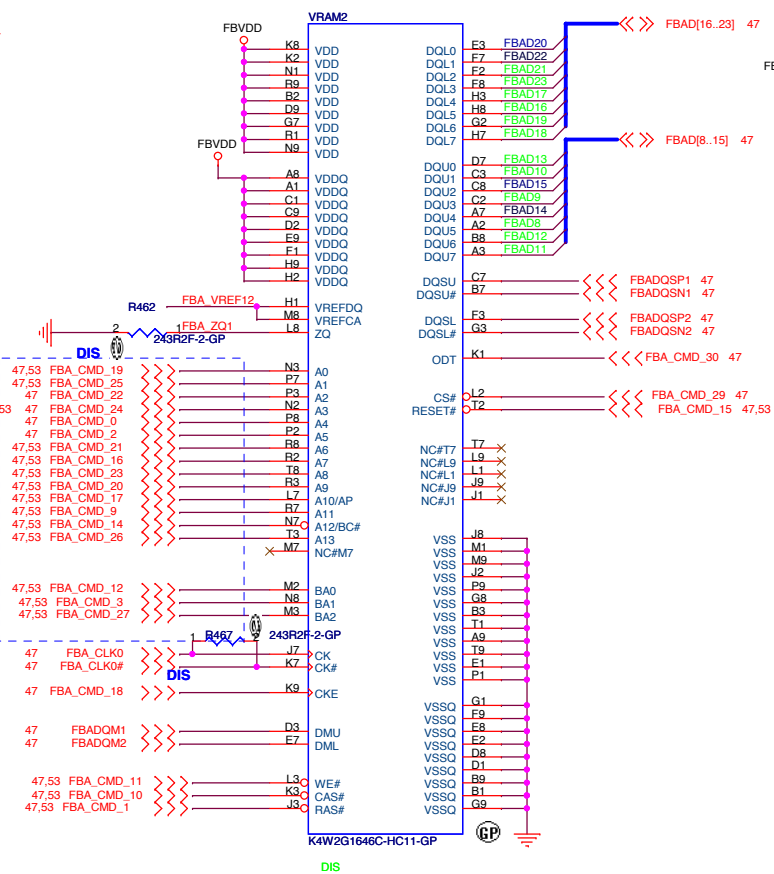
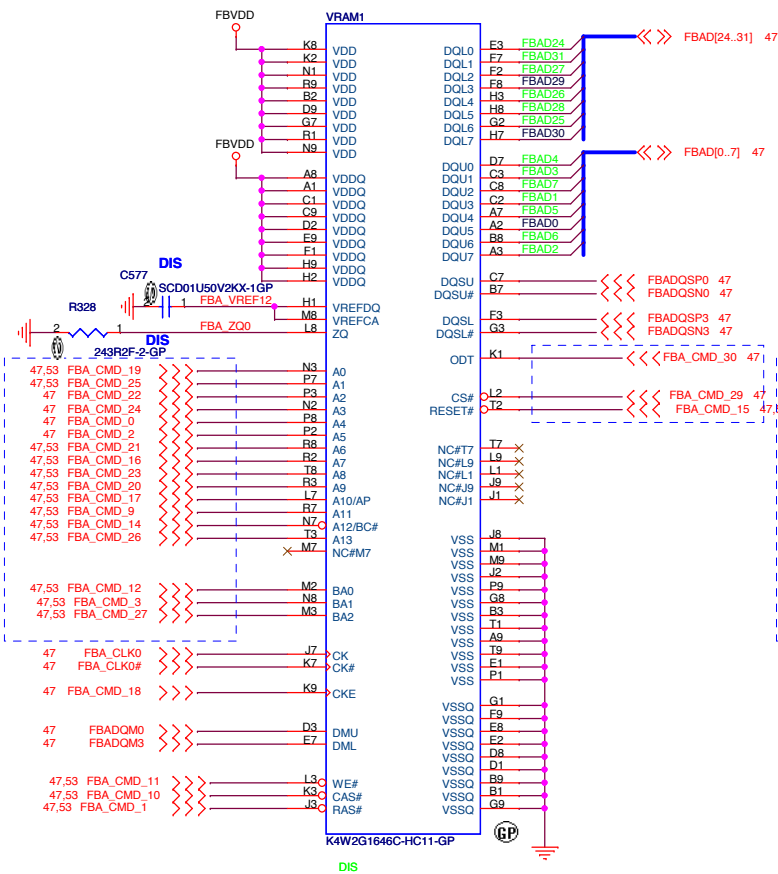


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Title		
N11M(3/6) DAC		
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